

## **MT9800xxxxx**

## **LCD** controller

## Hardware Reset and Power Sequence

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Document Revision History								
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### **Table of Contents**

	Confidentia
Table of Contents	
Document Revision History	2
Table of Contents	3
HW Design Note for Reset Circuit	4
Reset Circuit	
Power On and Reset Sequence	5
Exhibit 1 Terms and Conditions	7



# HW Design Note for Reset Circuit

#### **Reset Circuit**





#### **Power On and Reset Sequence**

## SOURCE External 3.3V LDO (or buck converter)+ External 1.5/1.8V LDO (or buck converter )+ External 0.95V LDO (or buck converter) + Reset

For external 3.3V LDO (or buck converter) + external 1.5/1.8V LDO (or buck converter) + external 0.95V LDO (or buck converter) + Reset, the timing is as Figure 1. The RST waveform must satisfy Table 1.



Figure 1: Correct Power Sequence for External 3.3V LDO or buck) + External 1.5/1.8V LDO (or buck) + External 0.95V LDO (or buck) + Reset

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Note 1: Timing for 3.3V set ready could lead or behind DDR power. t2 = Timing to 90%VDD

t3 = 3.3V/XTAL ready

Note 2: 3.3V Normal Power (AVDD\_EAR33, AVDD\_DPRX, AVDD\_DPTX, AVDD\_HDMIRX, AVDD\_ADC, AVDD\_AUSDM, AVDD\_PLL,

AVDD\_LPLL, AVDD\_MOD, AVDD\_USB, AVDD\_XTAL, VDDP, AVDD\_DPCRX, AVDD\_USB31C). 1.5/1.8V Normal power (AVDD\_DDR, VDDIO\_DRAM, VDD\_DRAM, AVDD\_MOD\_LDO). 0.95V Normal power (VDD, AVDDL\_DPRX, AVDDL\_HDMIRX, AVDDL\_DPTX, AVDDL\_DPCRX, AVDDL\_USB31CRX, AVDDL\_USB31CTX, AVDDL\_HUBRX, AVDDL\_HUBTX, DVDD\_NODIE, DVDD\_DDR, AVDDL\_MOD).



#### Figure 2: Reset Diagram

Table 1: Power & Reset Sequence

Parameter	Value	Unit
Txtal->rst	5	ms
VIH	2.0	V
VIL	0.9	V

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