LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT6711

HDMI2.0 to DP1.2 with Type-C

Datasheet

1. Features

- **HDMI2.0 Receiver**
  - Compliant to HDMI2.0 Standard
  - Support 3D Video Data Stream
  - Support HDCP1.4/2.2
  - Support HDR
  - Support Resolution up to 4Kx2K@60Hz
  - Support 8/10/12-bit Deep color
  - Support DDC and CEC
  - Support Hot-Plug Detect
  - Support Status and Control Data Channel (SCDC)
  - Support Data Lane Swap and Polarity Swap
  - Build-in Pattern Generation
- **DP1.2 Transmitter**
  - Compliant to VESA DP1.2 Standard
  - Support Four Lanes with 1.62Gbps (RBR), 2.7Gbps (HBR) or 5.4Gbps (HBR2) Data Rate
  - Support Resolution up to 4Kx2K@60Hz
  - Data Lane and Polarity Swapping
  - Support HDCP1.3 Encryption
  - Support 8/10/12-bit Deep Color
  - Support Hot-Plug Detect
  - Optional SSC 0.5% Down-Spreading Output
  - Configurable and Power-on-Calibrated Output Swing for Optimized EMI
  - Internal Rterm Calibration with Less than 5% Error
  - Support Backlight Control & MCCS over AUX for eDP
  - Support ASSR for eDP
  - Build-in Pattern Generation
- **Full-Featured USB Type-C**
  - Compatible with USB3.1 Gen1, USB Type-C R1.2, DP Alt Mode V1.0 and USB PD R3.0
  - 2 Data Roles Supported: DFP and UFP
  - 3 Power Roles Supported: SRC, SNK and DRP
  - USB PD-PHY (Tx/Rx) and BMC Encoding/Decoding
  - USB PD Protocol Control by Software
  - Bi-directional Active Switch for USB3.1 Gen1 SS Channel
  - USB Full-Featured, Orientation and Role Detection
  - 3-level Current Ability Advertise (Host Mode) or Detection (Device Mode) for Type-C Power: USB Default, 1.5A@5V, 3A@5V
  - Support FR_Swap
  - SBU Data Path Control for DP Alt Mode
  - Dead Battery Support When No Power Applied
  - Support Standby Mode for Low-Power Operating
- **USB Type-C Charging Port**
  - Compatible with USB Type-C R1.2 and USB PD R3.0
  - Only SNK Mode is Supported
  - Dead Battery Support When No Power Applied
- **Miscellaneous**
  - Support OSD display with 8K Programmable Dot Matrix and Attribute Table
  - 1.2V/1.8V/3.3V Supply Power
  - External 27MHz Crystal Reference Clock
  - Temperature Range: -40°C to +85°C
  - Packaged in BGA81 5mmx5mm, 7.5mmx7.5mm QFN64
  - Power Consumption: See Section 8.5

2. General Description

The Lontium LT6711 is HDMI2.0 to DP1.2 converter with internal Type-C Alternate Mode switch and PD controller.

For HDMI input, LT6711 features a HDMI2.0 receiver with 1 clock lane and 3 data lanes operating at maximum 6Gb/s per data lane and a maximum input bandwidth of 18Gb/s, allowing resolution up to 4Kx2K@60Hz for RGB format. The converter also integrates a DDC controller and supports both HDCP1.4 and HDCP2.2.

For DP1.2 output, it consists of 4 data lanes, supporting RBR (1.62Gbps), HBR (2.7Gbps) and HBR2 (5.4Gbps) link speeds. The build-in optional SSC function reduces EMI effect on EMI-concerned system application.

In order to be adaptable to the latest USB Type-C ecosystem, LT6711 integrates a high performance bi-directional Super-Speed switch controlled by CC logic and PD management unit to relieve mobile system design complexity and BOM cost. The switch function is compliant with VESA DP Alternate Mode on USB Type-C Standard.

The LT6711 is fabricated in advanced CMOS process and implemented in a small outline 5mmx5mm BGA81 (LT6711B) and 7.5mmx7.5mm QFN64 (LT6711A) package. This package is RoHS compliant and specified to operate from -40°C to +85°C.

3. Applications

- Mobile systems, VR/AR
- Cellular handsets, PAD/Tablets
- Digital video cameras and Digital still cameras

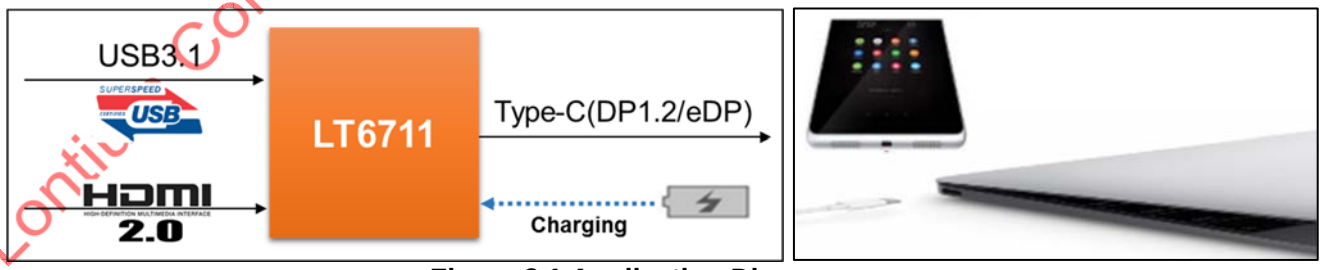

Figure 3.1 Application Diagrams

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT6711A	−40°C to +85°C	QFN64 (7.5*7.5)	Tray
LT6711B	−40°C to +85°C	BGA81 (5*5)	Tray

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5. Revision History

Version	Owner	Content	Date
R0.1	C T	Initial Release	07/19/2018
R0.2	C T	Add 1.8V Power Supply	07/24/2018
R0.3	C T	1. Add ASSR feature for eDP 2. Update BGA package ball assignment	11/21/2018
R0.4	C T	Add power consumption	05/23/2019
R0.5	C T	1. Update Figure 6.1.1 2. Fix pin direction and description for SSTXP/N	07/16/2019
R0.6	C T	Add Power On Sequence	07/24/2019
R0.7	C T	Update the parameters of storage temperature and ESD	09/18/2019
R0.8	C T, Z W	Update pin/ball name and descriptions for G3, G4, and G13~G18	11/25/2019

6. Pinning Information

6.1 Pin/Ball Configuration

To improve signal integrity, all differential pairs should be routed with 100Ω±10% differential impedance. Maximum trace length mismatch should be less than 5mil and keep total trace length to a minimum for all differential traces. Routing differential pairs on the top or bottom layer with no vias as on signal path is highly recommended.

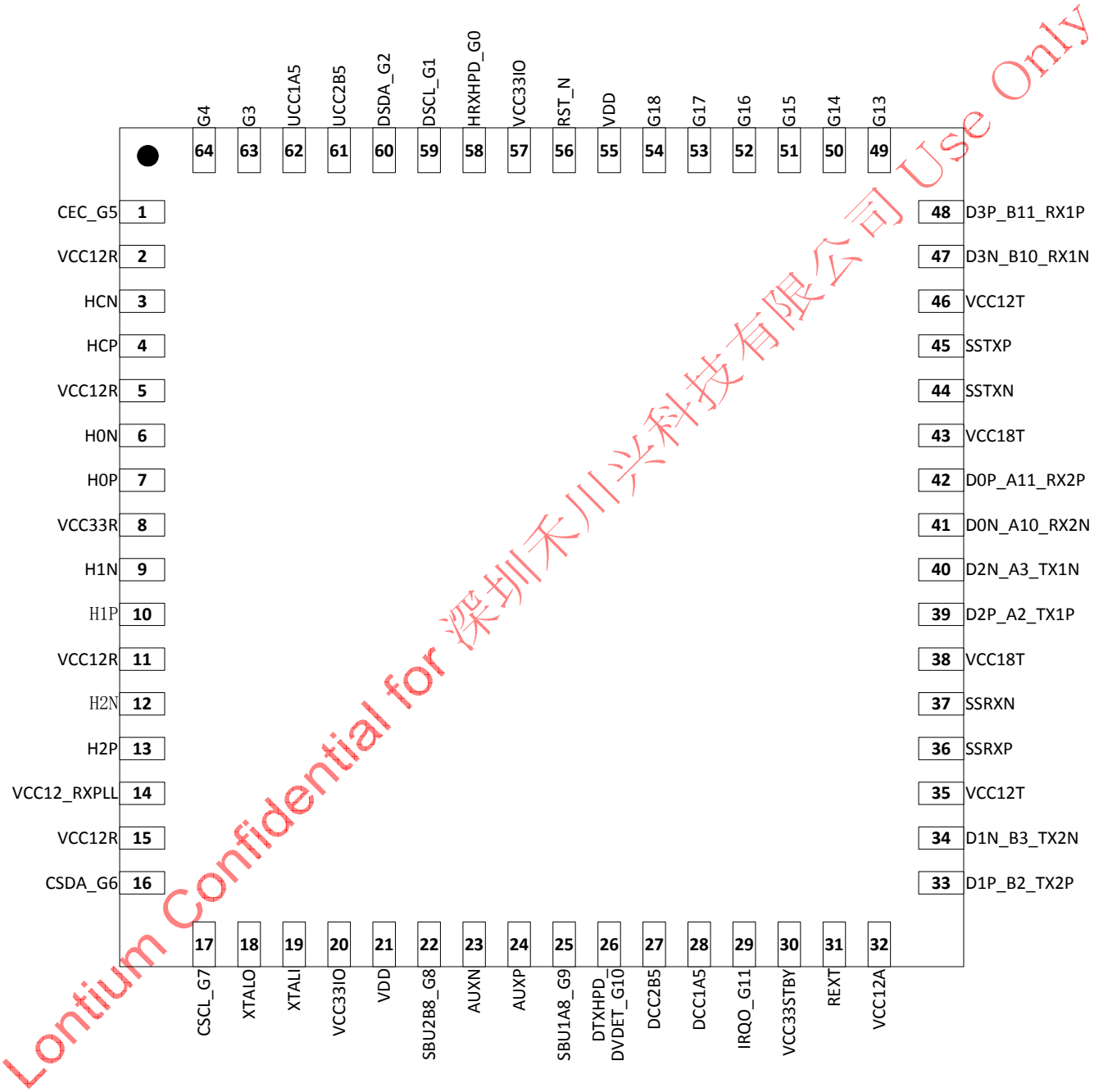


Figure 6.1.1 LT6711A (QFN64 7.5mm x 7.5mm) Pin Map (Top View)

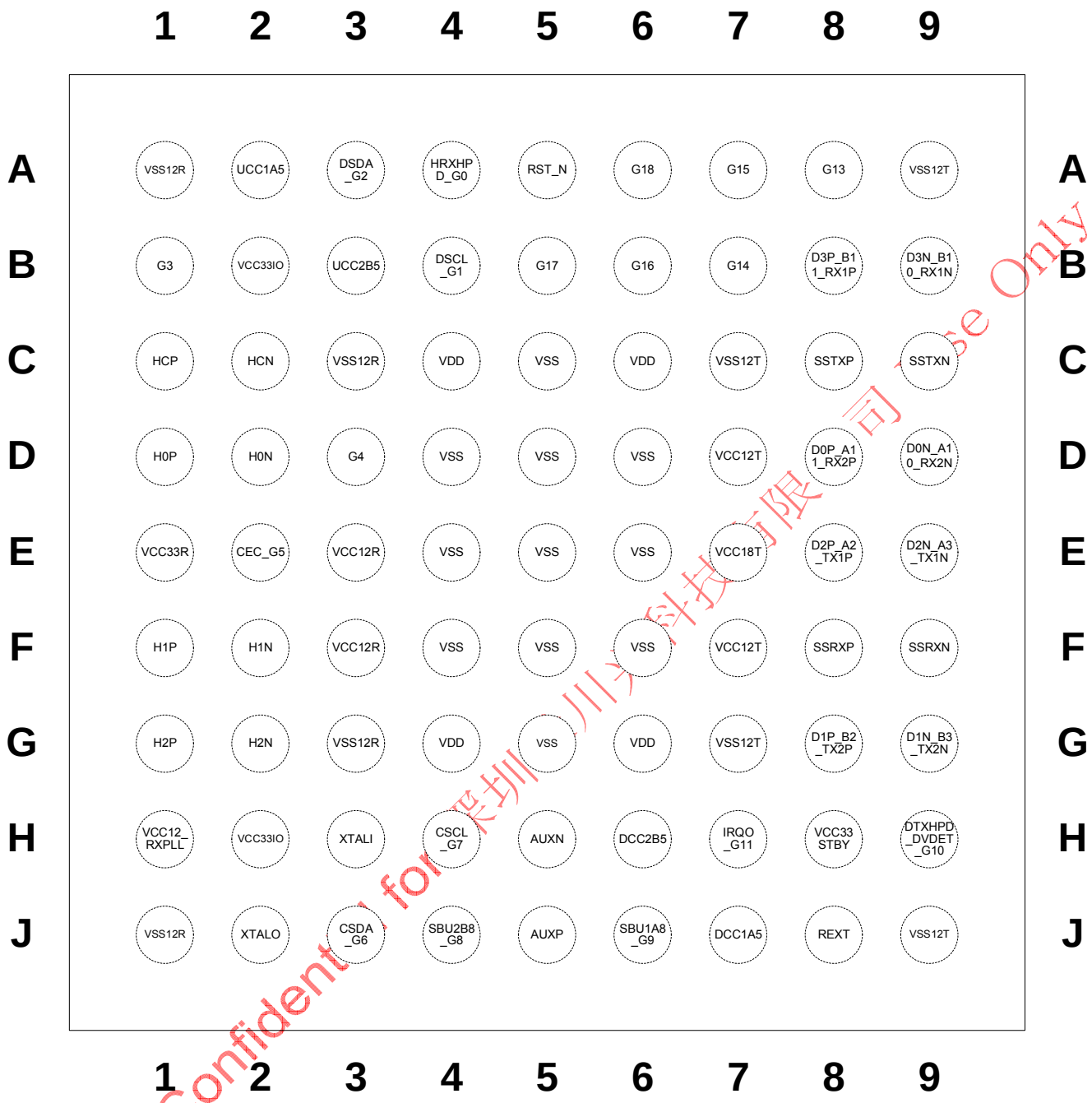


Figure 6.1.2 LT6711B (BGA81 5mm x 5mm) Ball Map (Top View)

For crystal oscillator, keep XTALI/XTALO as short as possible and away from noisy signal source. Minimize parasitic capacitances on these two pins and shield them with clean ground lines.

To minimize the power supply noise floor, at least one 0.1μF and one 0.01μF decoupling capacitor is recommended to be installed near all the LT6711 1.2V/1.8/3.3V power pins. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power inputs pins must be minimized.

6.2 Pin/Ball Description

Table 6.2.1 LT6711A Pin Description

Pin No.	Pin Name	Pin Description
1	CEC_G5	**HDMI CEC In/Out** Open-Drain Output and Schmitt Trigger Input. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
2	VCC12R	**Analog 1.2V Power** 1.2V power for analog.
3	HCN	**HDMIRX Clock Lane Negative Input** HDMIRX Negative input of clock differential pairs up to 300MHz.
4	HCP	**HDMIRX Clock Lane Positive Input** HDMIRX Positive input of clock differential pairs up to 300MHz.
5	VCC12R	**Analog 1.2V Power** 1.2V power for analog.
6	H0N	**HDMIRX Data Lane-0 Negative Input** HDMIRX Negative input of polarity swappable differential pairs up to 6Gb/s.
7	H0P	**HDMIRX Data Lane-0 Positive Input** HDMIRX Positive input of polarity swappable differential pairs up to 6Gb/s.
8	VCC33R	**Analog 3.3V Power** 3.3V power for analog.
9	H1N	**HDMIRX Data Lane-1 Negative Input** HDMIRX Negative input of polarity swappable differential pairs up to 6Gb/s.
10	H1P	**HDMIRX Data Lane-1 Positive Input** HDMIRX Positive input of polarity swappable differential pairs up to 6Gb/s.
11	VCC12R	**Analog 1.2V Power** 1.2V power for analog.
12	H2N	**HDMIRX Data Lane-2 Negative Input** HDMIRX Negative input of polarity swappable differential pairs up to 6Gb/s.
13	H2P	**HDMIRX Data Lane-2 Positive Input** HDMIRX Positive input of polarity swappable differential pairs up to 6Gb/s.
14	VCC12_RXPLL	**Analog 1.2V Power** 1.2V power for analog.
15	VCC12R	**Analog 1.2V Power** 1.2V power for analog.
16	CSDA_G6	**I2C Serial Clock Input** It serves as 5V tolerant serial port data IO slave for register access. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
17	CSCL_G7	**I2C Serial Clock Input** It serves as 5V tolerant serial port data clock slave for register access. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
18	XTALO	**Crystal Clock Output** A crystal oscillator should be attached between this pin and XTALI. If XTALI is used as reference clock input, this pin must be floating.
19	XTALI	**Crystal Clock Input** A crystal oscillator should be attached between this pin and XTALO. However, a CMOS 1.8/3.3V compatible clock signal can also be connected to this pin as reference clock.
20	VCC33IO	**IO/ESD 3.3V Power** 3.3V power for IO/ESD.
21	VDD	**Digital 1.2V Power** 1.2V power for digital core
22	SBU2B8_G8	**USB Type-C SBU2** Sideband Use Channel-2. An AC coupling capacitor is connected between this pin and AUXN. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
23	AUXN	**DPTX AUX Channel Negative In/Out** Negative in/out of AUX channel in DP mode. An AC coupling capacitor is connected between this pin and SBU2B8_G8.
24	AUXP	**DPTX AUX Channel Positive In/Out** Positive in/out of AUX channel in DP mode. An AC coupling capacitor is connected between this pin and SBU1A8_G9.

Pin No.	Pin Name	Pin Description
25	SBU1A8_G9	**USB Type-C SBU1** Sideband Use Channel-1. An AC coupling capacitor is connected between this pin and AUXP. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
26	DTXHPD_DVDET_G10	**DPTX HPD Input** DPTX hot-plug detect input in DP mode. **DCC VBUS Detect Input** VBUS Detect input for USB Type-C DCC port. A resistive voltage divider should be connected between this pin and VBUS. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
27	DCC2B5	**USB Type-C DCC Port Connector Configure Channel-2** CC2 or VCONN2 for USB Type-C DCC port. 5V tolerant.
28	DCC1A5	**USB Type-C DCC Port Connector Configure Channel-1** CC1 or VCONN1 for USB Type-C DCC port. 5V tolerant.
29	IRQO_G11	**Interrupt Request Output** In default, this pin is configured as 3.3V interrupt request (IRQ) output. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
30	VCC33STBY	**Analog 3.3V Power** 3.3V power for STBY mode operating.
31	REXT	**BandGap External Resistor** External 6K resistor for setting internal reference current.
32	VCC12A	**Analog 1.2V Power** 1.2V power for analog
33	D1P_B2_TX2P	**USB Type-C DCC Port Connector TX2 or DP Lane-1 Positive Output** USB Type-C positive output of polarity swappable differential pairs up to 5.4Gb/s.
34	D1N_B3_TX2N	**USB Type-C DCC Port Connector TX2 or DP Lane-1 Negative Output** TYPE-C negative output of polarity swappable differential pairs up to 5.4Gb/s.
35	VCC12T	**Analog 1.2V Power** 1.2V power for analog.
36	SSRXP	**USB3.1 Gen1 SSRX Positive Input** USB3.1 Gen1 SSRX positive input of differential pairs up to 5Gb/s (Connect to SSTX of USB3.1 Host).
37	SSRXN	**USB3.1 Gen1 SSRX Negative Input** USB3.1 Gen1 SSRX negative input of differential pairs up to 5Gb/s (Connect to SSTX of USB3.1 Host).
38	VCC18T	**Analog 1.8V Power** 1.8V power for analog.
39	D2P_A2_TX1P	**USB Type-C DCC Port Connector TX1 or DP Lane-2 Positive Output** USB Type-C positive output of polarity swappable differential pairs up to 5.4Gb/s.
40	D2N_A3_TX1N	**USB Type-C DCC Port Connector TX1 or DP Lane-2 Negative Output** USB Type-C negative output of polarity swappable differential pairs up to 5.4Gb/s.
41	D0N_A10_RX2N	**USB Type-C DCC Port Connector RX2 or DP Lane-0 Negative Output** USB Type-C negative output of polarity swappable differential pairs up to 5.4Gb/s.
42	D0P_A11_RX2P	**USB Type-C DCC Port Connector RX2 or DP Lane-0 Positive Output** USB Type-C positive output of polarity swappable differential pairs up to 5.4Gb/s.
43	VCC18T	**Analog 1.8V Power** 1.8V power for analog.
44	SSTXN	**USB3.1 Gen1 SSTX Negative Output** USB3.1 Gen1 SSTX negative output of differential pairs up to 5Gb/s (Connect to SSRX of USB3.1 Host).
45	SSTXP	**USB3.1 Gen1 SSTX Positive Output** USB3.1 Gen1 SSTX positive output of differential pairs up to 5Gb/s (Connect to SSRX of USB3.1 Host).
46	VCC12T	**Analog 1.2V Power** 1.2V power for analog.
47	D3N_B10_RX1N	**USB Type-C DCC Port Connector RX1 or DP Lane-3 Negative Output** USB Type-C negative output of polarity swappable differential pairs up to 5.4Gb/s.
48	D3P_B11_RX1P	**USB Type-C DCC Port Connector RX1 or DP Lane-3 Positive Output** USB Type-C positive output of polarity swappable differential pairs up to 5.4Gb/s.
49	G13	**GPIO In/Out** 5V tolerant GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
50	G14	**GPIO In/Out** 5V tolerant GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
51	G15	**GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.

Pin No.	Pin Name	Pin Description
52	G16	**GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
53	G17	**GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
54	G18	**UART Tx Debug Output** Uart Tx debug output pin. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
55	VDD	**Digital 1.2V Power** 1.2V power for digital core.
56	RST_N	**Hardware Reset Input** Chip reset signal. Active LOW.
57	VCC33IO	**IO/ESD 3.3V Power** 3.3V power for IO/ESD.
58	HRXHPD_G0	**HDMIRX HPD 5V Tolerant Output** HDMIRX hot-plug detect output. 5V tolerant. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
59	DSCL_G1	**HDMIRX DDC Clock Input** HDMIRX DDC serial clock input. 5V tolerant. **GPIO In/Out** 5V tolerant GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
60	DSDA_G2	**HDMIRX DDC Data Input/Output** HDMIRX DDC serial data input/output. 5V tolerant. **GPIO In/Out** 5V tolerant GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
61	UCC2B5	**USB Type-C UCC Port Connector Configure Channel-2** CC2 or VCONN2 for USB Type-C UCC port. 5V tolerant.
62	UCC1A5	**USB Type-C UCC Port Connector Configure Channel-1** CC1 or VCONN1 for USB Type-C UCC port. 5V tolerant.
63	G3	**GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
64	G4	**GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
65	#EPAD	**EPAD**

Table 6.2.2 LT6711B Ball Description

Ball No.	Ball Name	Pin Description
E1	VCC33R	**Analog 3.3V Power** 3.3V power for analog.
B2, H2	VCC33IO	**IO/ESD 3.3V Power** 3.3V power for IO/ESD.
H8	VCC33STBY	**Analog 3.3V Power** 3.3V power for STBY mode operating.
E3, F3	VCC12R	**Analog 1.2V Power** 1.2V power for analog.
A1, C3, G3, J1	VSS12R	**Analog 1.2V Ground** 1.2V ground for analog.
H1	VCC12_RXPLL	**Analog 1.2V Power** 1.2V power for analog.
D7, F7	VCC12T	**Analog 1.2V Power** 1.2V power for analog.
E7	VCC18T	**Analog 1.8V Power** 1.8V power for analog.
A9, C7, G7, J9	VSS12T	**Analog 1.2V Ground** 1.2V ground for analog.
C4, C6, G4, G6	VDD	**Digital 1.2V Power** 1.2V power for digital core
C5, D4, E4, F4 D5, E5, F5, D6, E6, F6, G5	VSS	**Digital 1.2V Ground** 1.2V ground for digital.
E2	CEC_G5	**HDMI CEC In/Out** Open-Drain Output and Schmitt Trigger Input. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
C2, C1	HCN, HCP	**HDMIRX Clock Lane Negative/Positive Input** HDMIRX Negative/Positive input of clock differential pairs up to 300MHz.
D2, D1	H0N, H0P	**HDMIRX Data Lane-0 Negative/Positive Input** HDMIRX Negative/Positive input of polarity swappable differential pairs up to 6Gb/s.
F2, F1	H1N, H1P	**HDMIRX Data Lane-1 Negative/Positive Input** HDMIRX Negative/Positive input of polarity swappable differential pairs up to 6Gb/s.
G2, G1	H2N, H2P	**HDMIRX Data Lane-2 Negative/Positive Input** HDMIRX Negative/Positive input of polarity swappable differential pairs up to 6Gb/s.
J3	CSDA_G6	**I2C Serial Clock Input** It serves as 5V tolerant serial port data IO slave for register access. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
H4	CSCL_G7	**I2C Serial Clock Input** It serves as 5V tolerant serial port data clock slave for register access. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
J2	XTALO	**Crystal Clock Output** A crystal oscillator should be attached between this pin and XTALI. If XTALI is used as reference clock input, this pin must be floating.
H3	XTALI	**Crystal Clock Input** A crystal oscillator should be attached between this pin and XTALO. However, a CMOS 1.8/3.3V compatible clock signal can also be connected to this pin as reference clock.
J4	SBU2B8_G8	**USB Type-C SBU2** Sideband Use Channel-2. An AC coupling capacitor is connected between this pin and AUXN. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
H5	AUXN	**DPTX AUX Channel Negative In/Out** Negative in/out of AUX channel in DP mode. An AC coupling capacitor is connected between this pin and SBU2B8_G8.
J5	AUXP	**DPTX AUX Channel Positive In/Out** Positive in/out of AUX channel in DP mode. An AC coupling capacitor is connected between this pin and SBU1A8_G9.

Ball No.	Ball Name	Pin Description
J6	SBU1A8_G9	**USB Type-C SBU1** Sideband Use Channel-1. An AC coupling capacitor is connected between this pin and AUXP. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
H9	DTXHPD_DVDET_G10	**DPTX HPD Input** DPTX hot-plug detect input in DP mode. **DCC VBUS Detect Input** VBUS Detect input for USB Type-C DCC port. A resistive voltage divider should be connected between this pin and VBUS. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
H6	DCC2B5	**USB Type-C DCC Port Connector Configure Channel-2** CC2 or VCONN2 for USB Type-C DCC port. 5V tolerant.
J7	DCC1A5	**USB Type-C DCC Port Connector Configure Channel-1** CC1 or VCONN1 for USB Type-C DCC port. 5V tolerant.
H7	IRQO_G11	**Interrupt Request Output** In default, this pin is configured as 3.3V interrupt request (IRQ) output. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
J8	REXT	**BandGap External Resistor** External 6K resistor for setting internal reference current.
G8, G9	D1P_B2_TX2P D1N_B3_TX2N	**USB Type-C DCC Port Connector TX2 or DP Lane-1 Positive/Negative Output** USB Type-C positive/negative output of polarity swappable differential pairs up to 5.4Gb/s.
F8, F9	SSRXP, SSRXN	**USB3.1 Gen1 SSRX Positive/Negative Input** USB3.1 Gen1 SSRX positive/negative input of differential pairs up to 5Gb/s (Connect to SSTX of USB3.1 Host).
E8, E9	D2P_A2_TX1P D2N_A3_TX1N	**USB Type-C DCC Port Connector TX1 or DP Lane-2 Positive/Negative Output** USB Type-C positive/negative output of polarity swappable differential pairs up to 5.4Gb/s.
D8, D9	D0P_A11_RX2P D0N_A10_RX2N	**USB Type-C DCC Port Connector RX2 or DP Lane-0 Positive/Negative Output** USB Type-C positive/negative output of polarity swappable differential pairs up to 5.4Gb/s.
C8, C9	SSTXP, SSTXN	**USB3.1 Gen1 SSTX Positive/Negative Output** USB3.1 Gen1 SSTX positive/negative output of differential pairs up to 5Gb/s (Connect to SSRX of USB3.1 Host).
B8, B9	D3P_B11_RX1P D3N_B10_RX1N	**USB Type-C DCC Port Connector RX1 or DP Lane-3 Positive/Negative Output** USB Type-C positive/negative output of polarity swappable differential pairs up to 5.4Gb/s.
A8	G13	**GPIO In/Out** 5V tolerant GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
B7	G14	**GPIO In/Out** 5V tolerant GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
A7	G15	**GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
B6	G16	**GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
B5	G17	**GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
A6	G18	**UART Tx Debug Output** Uart Tx debug output pin. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
A5	RST_N	**Hardware Reset Input** Chip reset signal. Active LOW.
A4	HRXHPD_G0	**HDMIRX HPD 5V Tolerant Output** HDMIRX hot-plug detect output. 5V tolerant. **GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
B4	DSCL_G1	**HDMIRX DDC Clock Input** HDMIRX DDC serial clock input. 5V tolerant. **GPIO In/Out** 5V tolerant GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.

Ball No.	Ball Name	Pin Description
A3	DSDA_G2	**HDMIRX DDC Data Input/Output** HDMIRX DDC serial data input/output. 5V tolerant. **GPIO In/Out** 5V tolerant GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
B3	UCC2B5	**USB Type-C UCC Port Connector Configure Channel-2** CC2 or V_{CONN2} for USB Type-C UCC port. 5V tolerant.
A2	UCC1A5	**USB Type-C UCC Port Connector Configure Channel-1** CC1 or V_{CONN1} for USB Type-C UCC port. 5V tolerant.
B1	G3	**GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.
D3	G4	**GPIO In/Out** 3.3V GPIO for debug purpose. It can be configured as: push-pull output with 2-level driving capability, open-drain output, 100K pull-up, 100K pull-down and GPI.

7. Function Block Diagram

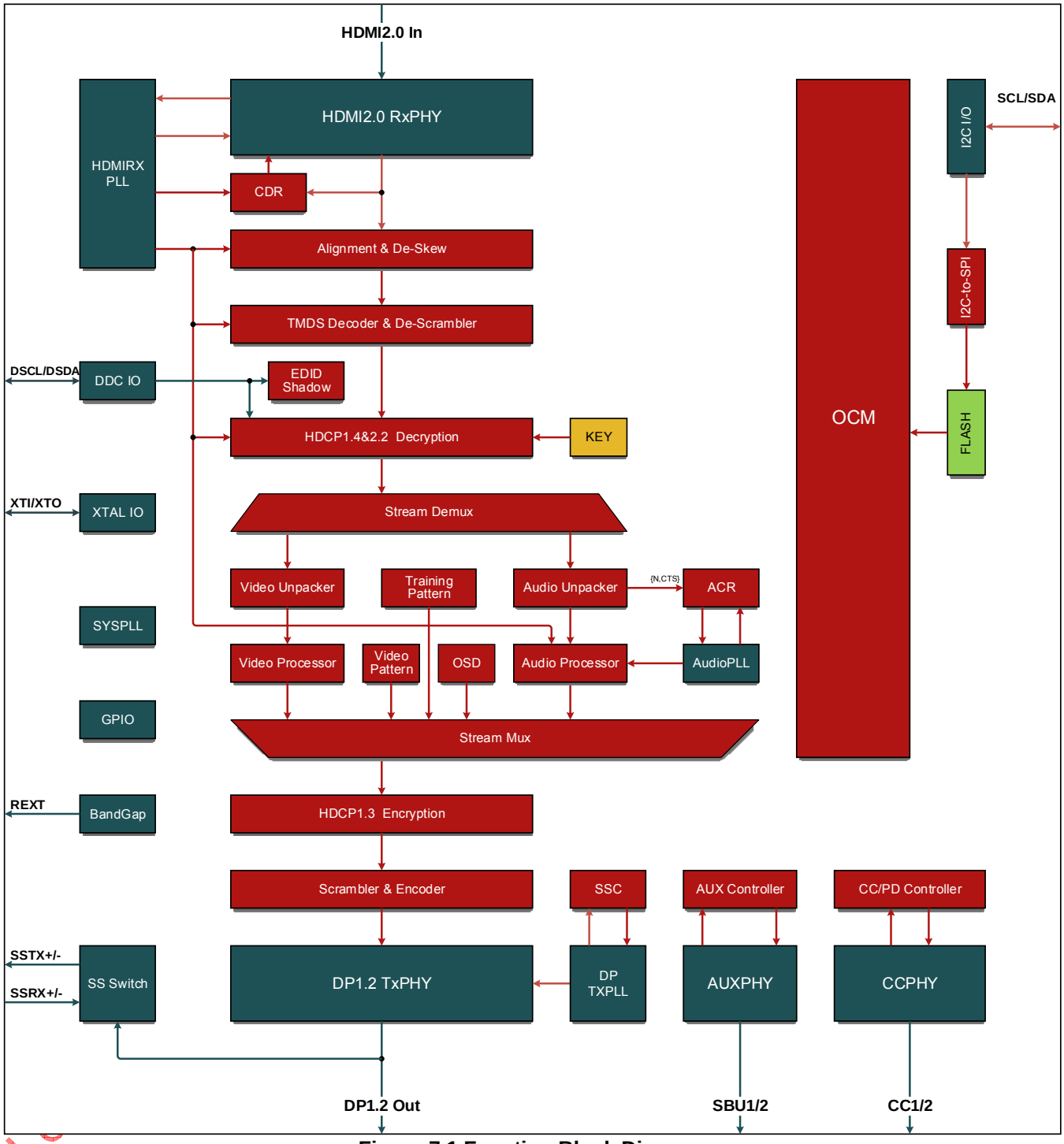


Figure 7.1 Function Block Diagram

8. Electrical Characteristics

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC12R, VCC12_RXPLL VCC12A, VCC12T, VDD	1.2V Power Supply Voltage	-0.3		1.32	V
VCC18T	1.8V Power Supply Voltage	-0.3		1.98	V
VCC33IO, VCC33R, VCC33STBY	3.3V Power Supply Voltage	-0.3		3.6	V
V_I	CMOS Terminal Input Voltage Range	-0.3		3.6	V
V_O	CMOS Terminal Output Voltage Range	-0.3		3.6	V
T_S	Storage Temperature	-60		140	℃
ESD	HBM Elastrostatic Discharge Level		2000		V

Notes:
1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Function operation should be restricted to the conditions described under Normal Operating Conditions.

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC12R, VCC12_RXPLL VCC12A, VCC12T, VDD	1.2V Power Supply Voltage	1.15	1.2	1.32	V
VCC18T	1.8V Power Supply Voltage	1.62	1.8	1.98	V
VCC33IO, VCC33R, VCC33STBY	3.3V Power Supply Voltage	3.0	3.3	3.6	V
VCC_N	Power Supply Voltage Noise			50	mV
T_A	Operating Free-air Temperature	-40	27	85	℃

8.3 DC Characteristics

Table 8.3.1 DC Characteristics

HDMI Receiver DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
Vidiff	Input differential voltage level			1.2	V
Vicm	Input common mode voltage,if sink supports only<=165MHz	AVCC-300m		AVCC-37.5m	mV
	Input common mode voltage,if sink supports >165MHz	AVCC-400m		AVCC-37.5m	mV
AVCC	Termination supply voltage	3.3±5%			V
RT	Termination resistance	50±5%			Ω
DP Transmitter DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
Vbias_TX	TX DC Bias Voltage	0		2	V
Vtx_ac_cm_hbr2	TX AC Common Mode Voltage			20	mVrms

Vtx_ac_cm_hbr2	TX AC Common Mode Voltage			30	mVrms
Vtx_diff_vpp_level0	Differential Peak to Peak Output Swing Level0	0.34	0.4	0.46	V
Vtx_diff_vpp_level1	Differential Peak to Peak Output Swing Level1	0.51	0.6	0.68	V
Vtx_diff_vpp_level2	Differential Peak to Peak Output Swing Level2	0.69	0.8	0.92	V
Vtx_pre_emp_ratio	Pre-emphasis level 0	0	0	0	dB
	Pre-emphasis level 1	2.8	3.5	4.2	dB
	Pre-emphasis level 2	4.8	6	7.2	dB
	Pre-emphasis level 3	7.5	9.5	11.4	dB
Ctx	AC couple capacitance	75		200	nF
TX_SHORT	TX short circuit current limit			50	mA
RTX_DIFF	Differential Impedance	80	100	120	Ω
TYPE-C Switch DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
Vterm	Termination voltage range at input / output	0		2	V

8.4 AC Characteristics

Table 8.4.1 AC Characteristics

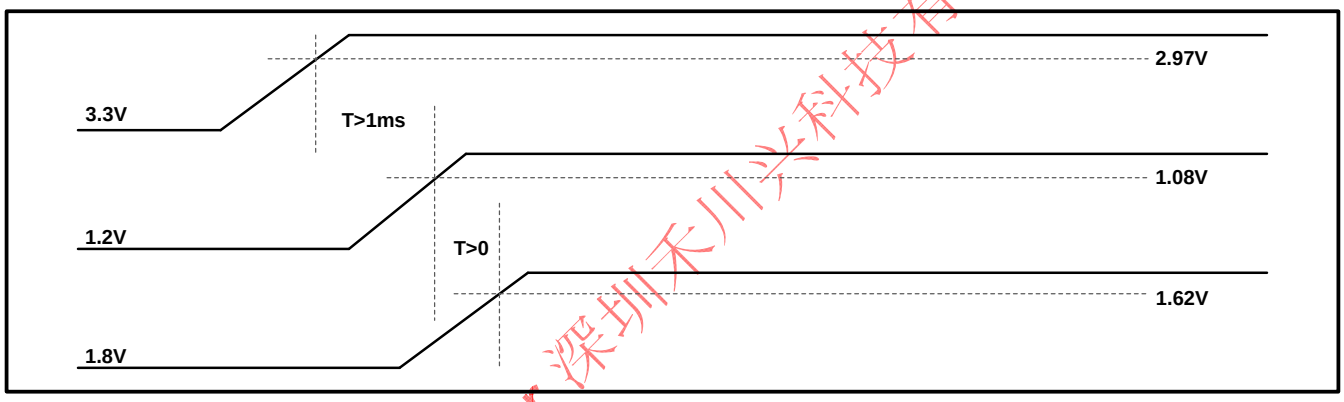
HDMI Receiver AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
Vidiff	Input differential voltage	150		1560	mV
Intra-Pair Skew	Skew between differential pair,TMDS clock below 222.75MHz			0.4Tbit	
	Skew between differential pair,TMDS clock above 222.75MHz			0.15Tbit+112ps	
Inter-Pair Skew	Skew between different channel			0.2Tcharacter+1.78ns	
TJitter	TMDS clock jitter			0.3Tbit	
DP Transmitter AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
Ttx_eye_chip_HBR2	Minimum TX eye width at pkg pin	0.73			UI
Ttx_jitter_HBR2	Maximum time between the jitter median and maximum deviation from the median at TX pkg pin			0.135	UI
Ttx_eye_chip_HBR	Minimum TX eye width at pkg pin	0.72			UI
Ttx_jitter_HBR	Maximum time between the jitter median and maximum deviation from the median at TX pkg pin			0.147	UI
Ttx_eye_chip_RBR	Minimum TX eye width at pkg pin	0.82			UI
Ttx_jitter_RBR	Maximum time between the jitter median and maximum deviation from the median at TX pkg pin			0.09	UI
Ttx_rise_chip Ttx_fall_chip	D+/D- TX output rise and fall time at TX pkg pins	50		130	ps
RL_TX_DIFF	Differential Return Loss at 0.675Ghz at TX pkg pins	12			dB
	Differential Return Loss at 1.35Ghz at TX pkg pins	9			dB
Ttx_skew	Lane intra pair output skew at pkg pins			20	ps
Ttx_rise_fall	Lane intra pair rise and fall time mismatch at pkg ins			5	%

TYPE-C Switch AC Specifications					
Symbol	Parameter	Min	Typ	Max	Unit
IL@2.5GHz	Insertion Loss at 5.0Gb/s (USB3.1 Gen1)			2.45	dB
RL@2.5GHz	Return Loss at 5.0Gb/s (USB3.1 Gen1)	9			dB
OI@2.5GHz	Off Isolation at 5.0Gb/s (USB3.1 Gen1)	22			dB

8.5 Power Consumption

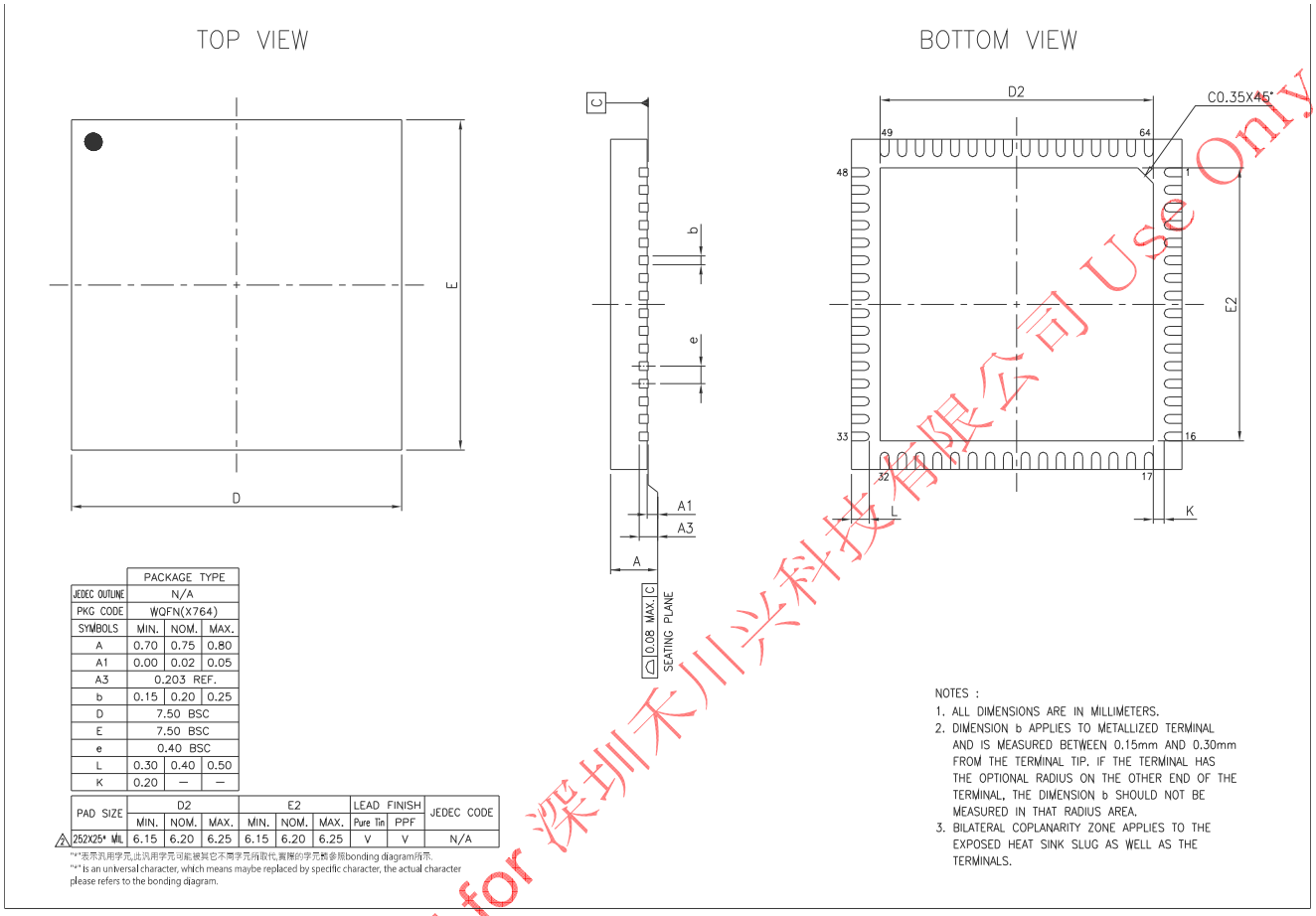
Resolution	Number of DP Lanes	Data Rate	VCC33 (mA)	VCC18 (mA)	VCC12 (mA)
4K60	4	5.4Gb/s	108	95	624
4K30	2	5.4Gb/s	97	32	408
1080P	1	5.4Gb/s	55	16	297

8.6 Power On Sequence



9. Package Information

The LT6711 is available in QFN64 7.5mm x 7.5mm (LT6711A) package with exposed pad (E-PAD 6.2mm*6.2mm) and in BGA81 5mm x 5mm (LT6711B) package. E-PAD incorporates features that provide a very low thermal resistance path for heat removal from the IC. The E-PAD on the device must be soldered to the PCB ground plane for proper electrical and thermal performance.



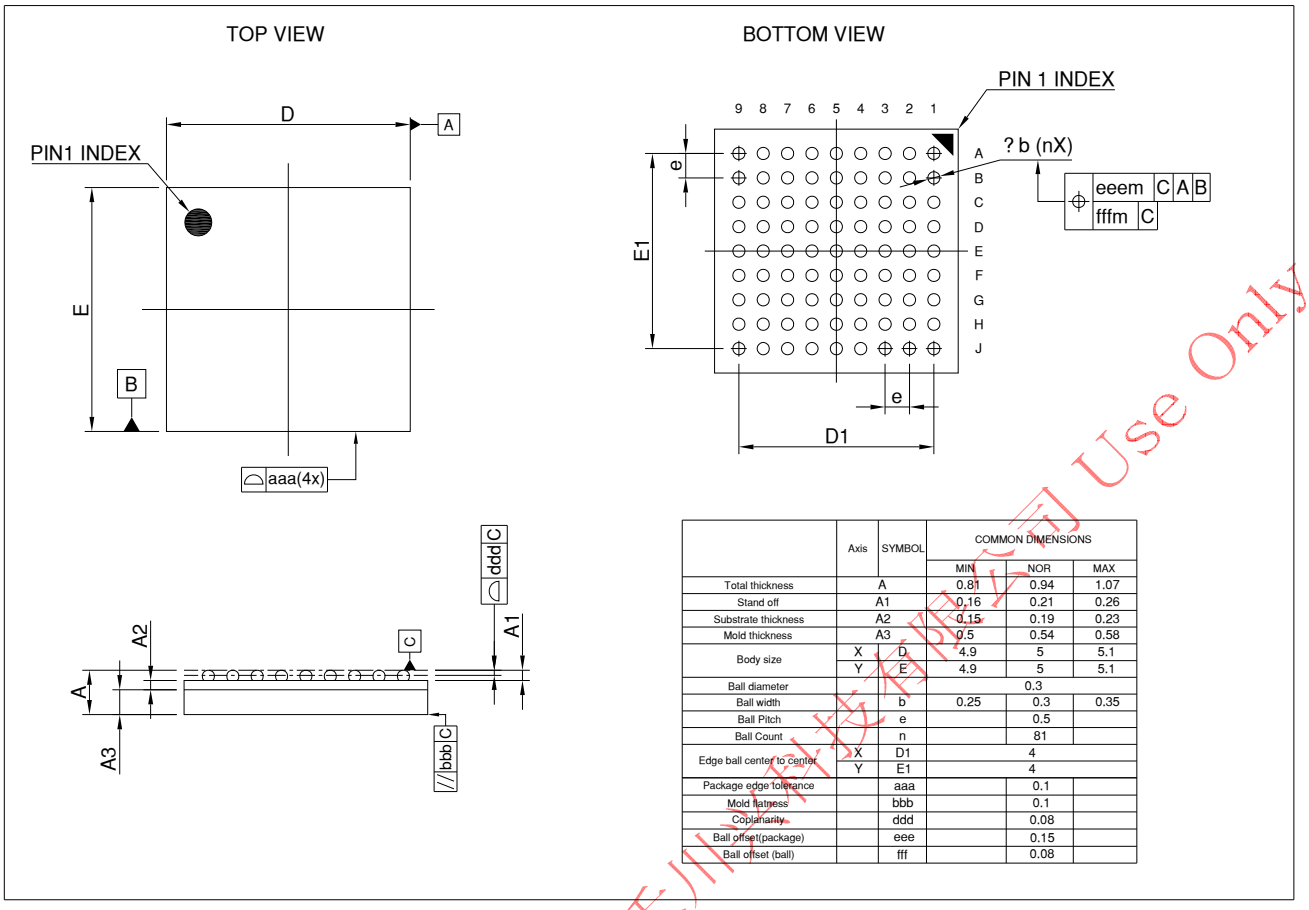
	PACKAGE TYPE		
JEDEC OUTLINE	N/A		
PKG CODE	WQFN(X764)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	7.50 BSC		
E	7.50 BSC		
e	0.40 BSC		
L	0.30	0.40	0.50
K	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
⚠ 252X25* MIL	6.15	6.20	6.25	6.15	6.20	6.25	V	V	N/A

"*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元視參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 9.1 LT6711A QFN64 7.5mmx7.5mm Package



	Axis	SYMBOL	COMMON DIMENSIONS		
			MIN	NOR	MAX
Total thickness		A	0.81	0.94	1.07
Stand off		A1	0.16	0.21	0.26
Substrate thickness		A2	0.15	0.19	0.23
Mold thickness		A3	0.5	0.54	0.58
Body size	X	D	4.9	5	5.1
	Y	E	4.9	5	5.1
Ball diameter				0.3	
Ball width		b	0.25	0.3	0.35
Ball Pitch		e		0.5	
Ball Count		n		81	
Edge ball center to center	X	D1		4	
	Y	E1		4	
Package edge tolerance		aaa		0.1	
Mold flatness		bbb		0.1	
Coplanarity		ddd		0.08	
Ball offset(package)		eee		0.15	
Ball offset (ball)		fff		0.08	

Figure 9.2 LT6711B BGA81 5mmx5mm Package

Visit our corporate web page at: www.lontiumsemi.com
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Sales: sales@lontium.com