Application Note: AN_SY8089/SY8089A

High Efficiency 5.5V, 2A continuous, 3A peak, 1MHz Synchronous Step Down Regulator

General Description

The SY8089 and SY8089A are high-efficiency, high frequency synchronous step-down DC-DC regulator IC capable of delivering up to 2A output current. The SY8089 and SY8089A operate over a wide input voltage range from 2.7V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Low output voltage ripple and small external inductor and capacitor sizes are achieved with greater than 1MHz switching frequency.

SY8089 integrates short circuit and over-voltage latch off protection.

Ordering Information

SY8089 □(□□)□
Temperature Code
Package Code
Optional Spec Code

Ordering Number	Package type	Note
SY8089AAC	SOT23-5	
SY8089AAAC	SOT23-5	

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom):110mΩ/80mΩ
- 2.7-5.5V input voltage range
- 2A continuous, 3A peak load current capability
- 1MHz switching frequency minimizes the external components
- Internal softstart limits the inrush current
- Reliable short circuit protection:
  - ○ SY8089: Latch off protection
  - ○ SY8089A: Hic-cup mode protection
- Reliable over-voltage protection:
  - ○ SY8089: Latch off protection
  - ○ SY8089A: No latch off protection
- 100% dropout operation
- RoHS Compliant and Halogen Free
- Compact package: SOT23-5

Applications

- LCD TV
- Set Top Box
- Net PC
- Mini-Notebook PC
- Access Point Router

Typical Applications

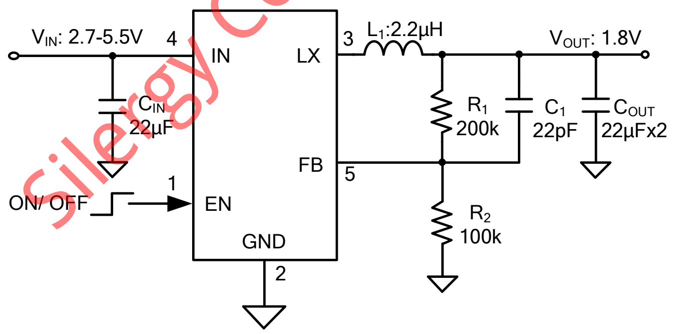


Figure 1.Schematic diagram

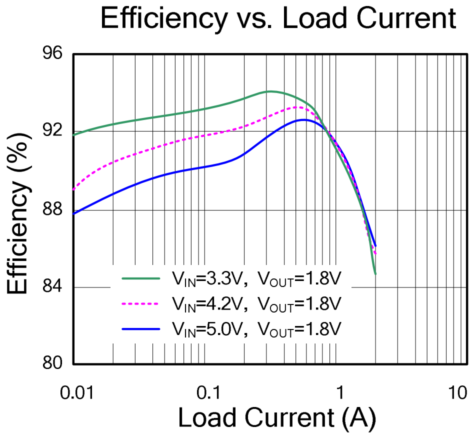
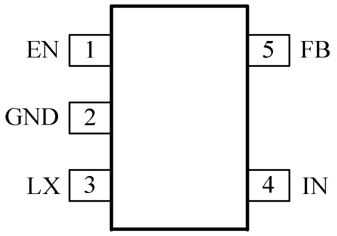


Figure 2. Efficiency vs Load Current

Pinout (top view)



SOT23-5

Part Number	Package type	Top Mark①
SY8089AAC	SOT23-5	***JX**xyz*
SY8089AAAC	SOT23-5	***KV**xyz*

Note①: x=year code, y=week code, z= lot number code

Pin Name	Pin Number	Pin Description
EN	1	Enable control. Pull high to turn on. Do not float.
GND	2	Ground pin.
LX	3	Inductor pin. Connect this pin to the switching node of inductor.
IN	4	Input pin. Decouple this pin to GND pin with at least 10μF ceramic cap.
FB	5	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{out}=0.6*(1+R_1/R_2)$.

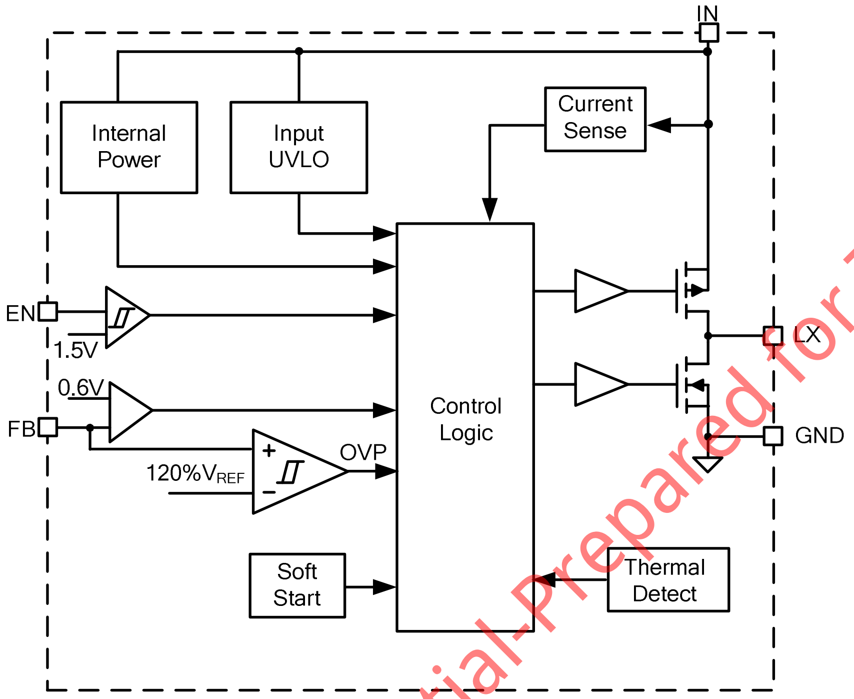
Absolute Maximum Ratings (Note 1)

Supply Input Voltage	-0.3V to 6.0V
Enable, FB Voltage	-0.3V to V_{IN} + 0.6V
Power Dissipation, P_D @ T_A = 25°C,	
SOT23-5	0.6W
Package Thermal Resistance (Note 2)	
θ_{JA}	170°C/W
θ_{JC}	130°C/W
Junction Temperature Range	-40°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C

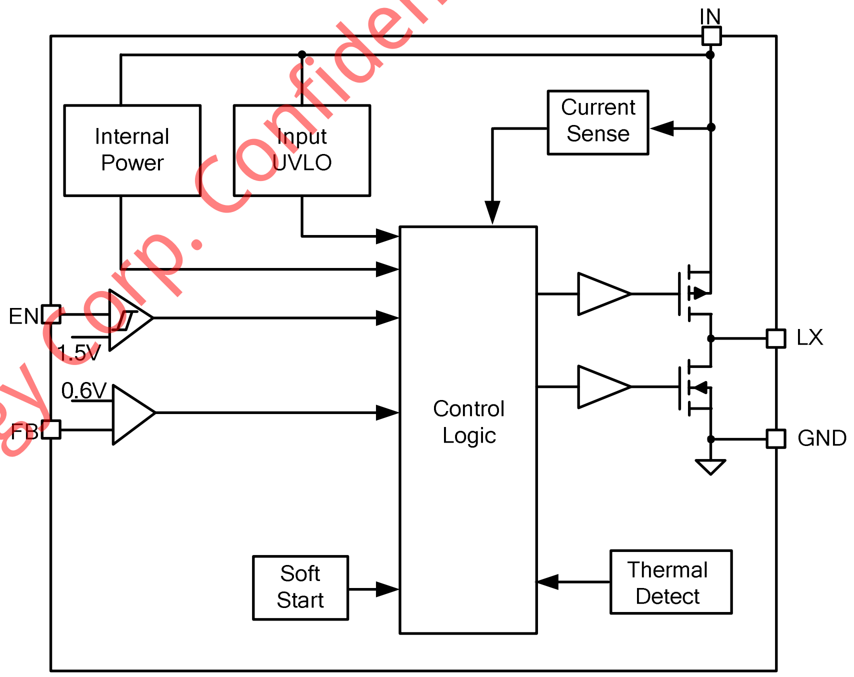
Recommended Operating Conditions (Note 3)

Supply Input Voltage	2.7V to 5.5V
Junction Temperature Range	-40°C to 125°C
Ambient Temperature Range	-40°C to 85°C

Block Diagram


IN
Internal Power
Input UVLO
Current Sense
EN
1.5V
0.6V
FB
120%VREF
OVP
Control Logic
LX
GND
Soft Start
Thermal Detect

(SY8089)


IN
Internal Power
Input UVLO
Current Sense
EN
1.5V
0.6V
FB
Control Logic
LX
GND
Soft Start
Thermal Detect

(SY8089A)

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 2.5V, L = 2.2µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise specified)

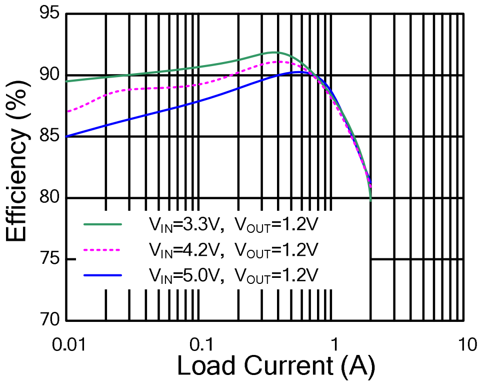
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.7		5.5	V
Quiescent Current	I_Q	IOUT=0, VFB=VREF · 105%	35	55	65	µA
Shutdown Current	I_{SHDN}	EN=0		0.1	1	µA
Feedback Reference Voltage	V_{REF}		0.588	0.6	0.612	V
FB Input Current	I_{FB}	VFB=VIN	-50		50	nA
PFET RON	$R_{DS(ON),P}$		85	110	125	mΩ
NFET RON	$R_{DS(ON),N}$		65	80	90	mΩ
PFET Current Limit	I_{LIM}		3.5		4.8	A
EN rising threshold	V_{ENH}		1.5			V
EN falling threshold	V_{ENL}				0.4	V
Input UVLO threshold	V_{UVLO}				2.65	V
UVLO hysteresis	V_{HYS}			0.2		V
Oscillator Frequency	F_{OSC}	IOUT=500mA	0.85	1	1.15	MHz
Short Circuit Protection Latch Off Threshold	V_{SCP}			0.25		V
Min ON Time				75		ns
Max Duty Cycle			100			%
Soft Start Time	T_{SS}			1.2		ms
Output Discharge Switch On Resistance	R_{DISCH}		35	50	65	Ω
Thermal Shutdown Temperature	T_{SD}			160		°C

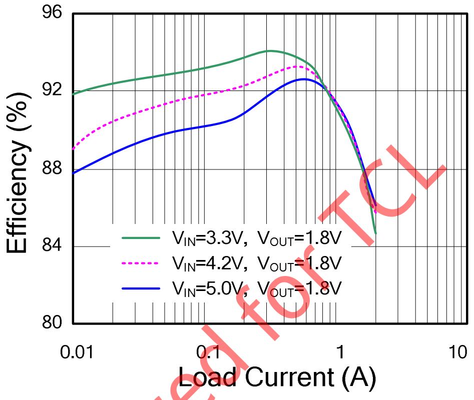
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

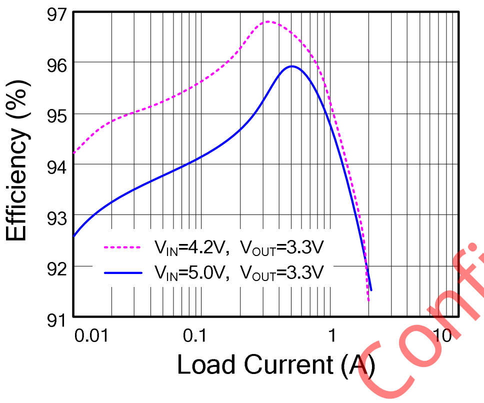
Note 2: Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

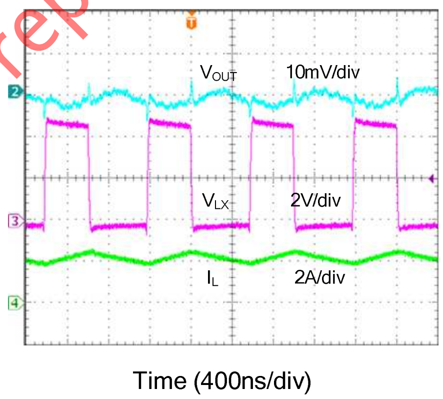
Note 3: The device is not guaranteed to function outside its operating conditions.

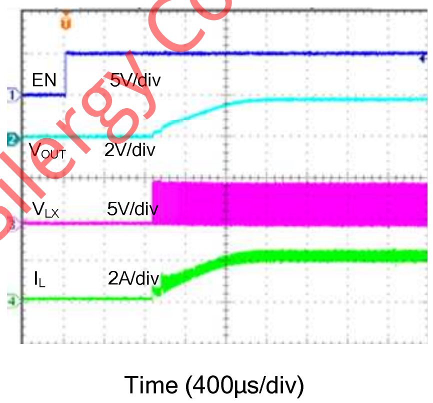
Typical Performance Characteristics

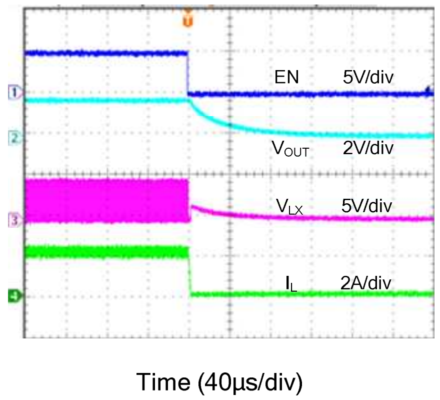

Efficiency vs. Load Current


Efficiency vs. Load Current


Efficiency vs. Load Current

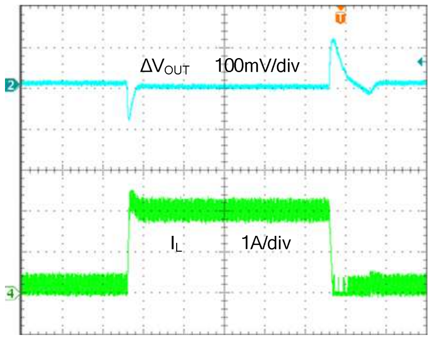

Output Ripple
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=2A)


Startup from Enable
(V_{IN}=5.0V, V_{OUT}=1.8V,I_{LOAD}=2.0A)


Shutdown from Enable
(V_{IN}=5.0V, V_{OUT}=1.8V,I_{LOAD}=2.0A)

Load Transient

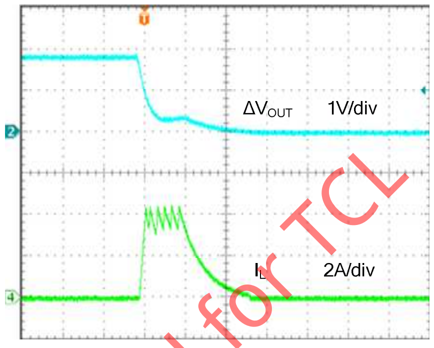
(V_{IN}=5.0V, V_{OUT}=1.8V,I_{LOAD}=0.2-2.0A)



Time (40µs/div)

Short Circuit Protection

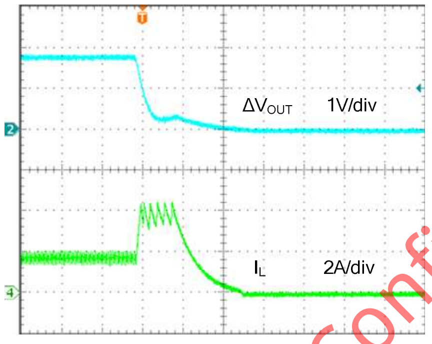
(V_{IN}=5.0V, V_{OUT}=1.8V,I_{LOAD}=0A-Short)



Time (20µs/div)

Short Circuit Protection

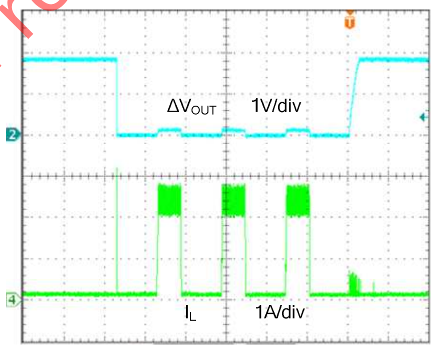
(V_{IN}=5.0V, V_{OUT}=1.8V,I_{LOAD}=2.0A-Short)



Time (20µs/div)

Short Circuit Protection

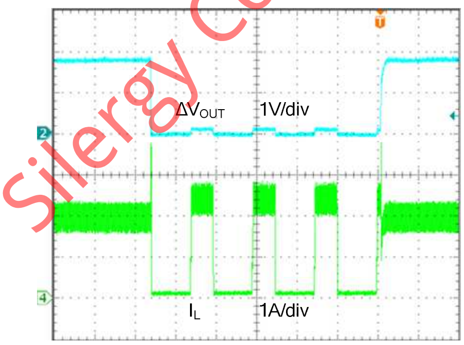
(V_{IN}=5.0V, V_{OUT}=1.8V,I_{LOAD}=0A-Short, SY8089A)



Time (4ms/div)

Short Circuit Protection

(V_{IN}=5.0V, V_{OUT}=1.8V,I_{LOAD}=2.0A-Short, SY8089A)



Time (4ms/div)

Operation Principle

SY8089 is a synchronous buck regulator IC that integrates the PWM control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low $R_{DS(ON)}$ power switches and proprietary PWM control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

Short Circuit Protection

（SY8089）After the soft start is over, if the output voltage falls below 40% of the regulation level, IC will turn off both power switches, entering short circuit protection. It will remain in this state until the IN or EN voltage is recycled.

(SY8089A) The frequency is folded back to about 30% of the nominal frequency and the current limit is folded back to 3.0A to prevent the inductor current from runaway and to reduce the power dissipation of the IC under short circuit conditions.

Over-voltage Protection

If the output voltage exceeds 120% of the regulation level for more than 20µs, IC will turn off both power switches and turn on the discharge switch, entering over-voltage protection. It will remain in this state until IN or EN voltage is recycled.

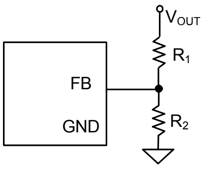
Applications Information

Because of the high integration in the SY8089 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors (R1 and R2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R1 and R2:

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10k and 1M is highly recommended for both resistors. If Vout is 1.8V, R1=100k is chosen, then R2 can be calculated to be 50k.:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1(\Omega).$$



Input capacitor C_{IN}:

This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

This formula has a maximum at $V_{IN}=2V_{OUT}$ condition, where $I_{CIN\_RMS}=I_{OUT}/2$. This simple worst-case condition is commonly used for DC/DC design.

With the maximum load current at 2.0A. A typical X5R or better grade ceramic capacitor with 6.3V rating and more than 1 pcs 22µF capacitor can handle this ripple current well. To minimize the potential noise problem, ceramic capacitor should really be placed close to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6.3V rating and greater than 22µF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY8089 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{OUT,\,MAX} + \frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{2\cdot F_{SW}\cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shut down mode, the SY8089 shutdown current drops to lower than 0.1uA. Driving the EN pin high (>1.5V) will turn on the IC again.

Load Transient Considerations:

The SY8089 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF ceramic cap in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

Layout Design:

The layout design of SY8089 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, L, R_1 and R_2.

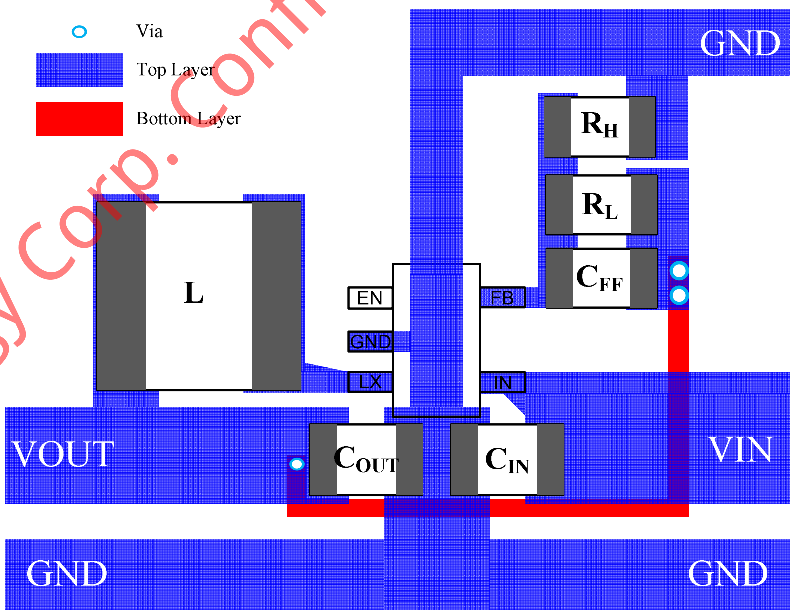
1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

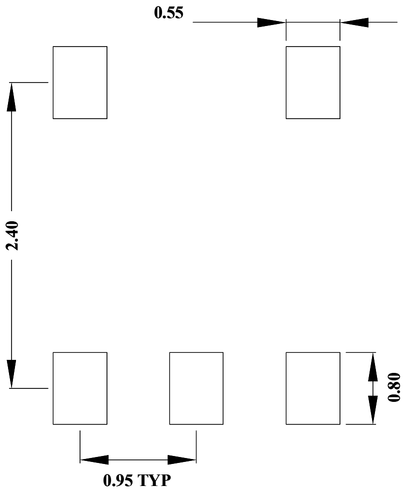
3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The components R_1, R_2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

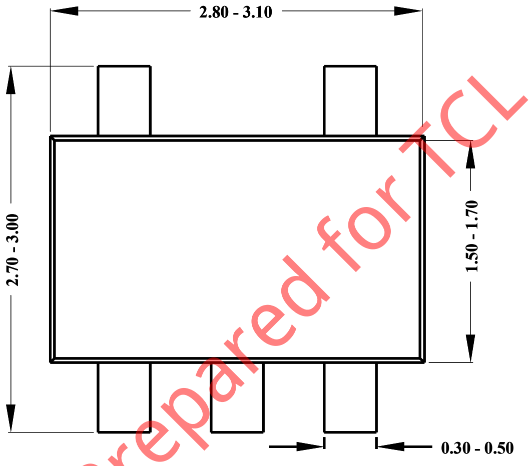
5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a LiIon battery, it is desirable to add a pull down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

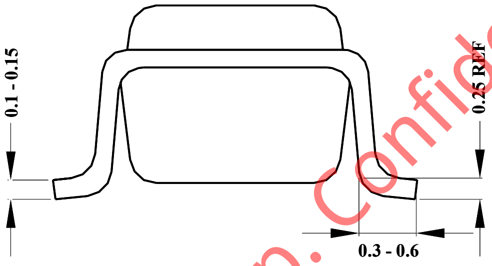


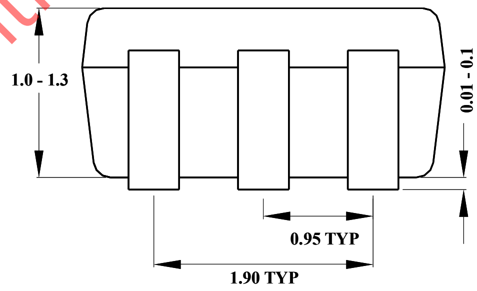
SOT23-5 Package outline & PCB layout design


0.55
2.40
0.80
0.95 TYP

Recommended Pad Layout


2.80 - 3.10
2.70 - 3.00
1.50 - 1.70
0.30 - 0.50


0.1 - 0.15
0.25 REF
0.3 - 0.6

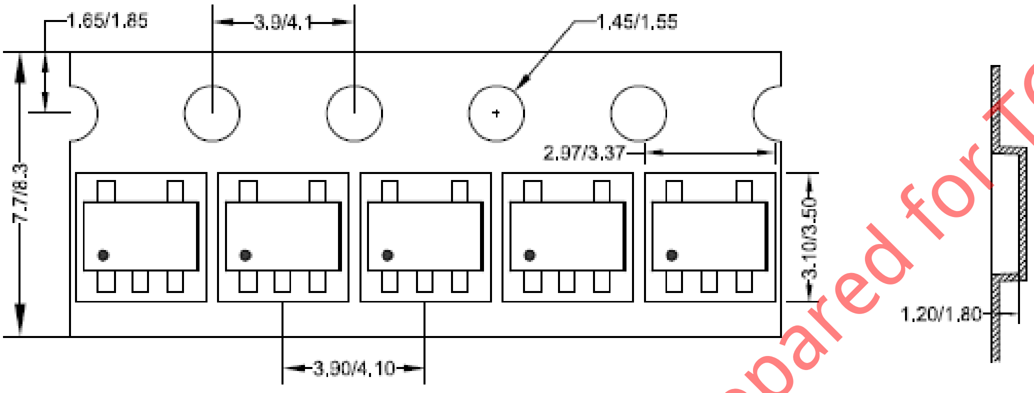

1.0 - 1.3
0.01 - 0.1
0.95 TYP
1.90 TYP

Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

Taping & Reel Specification

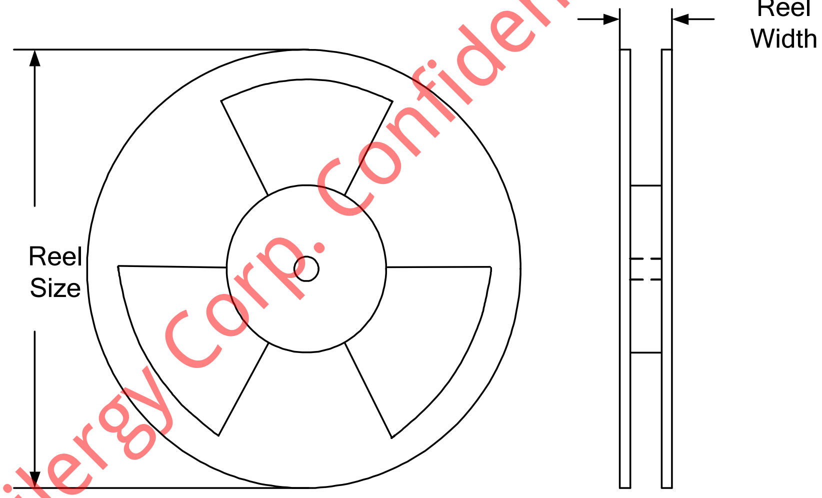
1. Taping orientation

SOT23-5


1.65/1.85
3.9/4.1
1.45/1.55
2.97/3.37
7.7/8.3
3.10/3.50
1.20/1.80
3.90/4.10

Feeding direction →

2. Carrier Tape & Reel specification for packages


Reel Width
Reel Size

Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-5	8	4	7"	8.4	280	160	3000

3. Others: NA