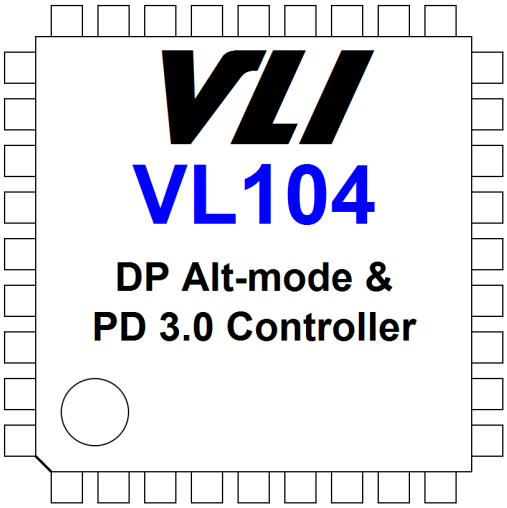
VIA Labs, Inc.

Datasheet

VL104
DP Alt-mode & PD 3.0 Controller with Buck Controller

March 30th, 2018

Revision 0.80



Revision History

Rev	Date	Note	Initial
0.80	03/30/2018	Preliminary release	HC

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Product Features

VL104

DisplayPort Alt-mode & PD 3.0 Controller with Buck Controller for USB-C Devices

■**CC Logic & PD 3.0 Engine** supporting one charging UFP and two DRP DFPs
– Compliant to USB Type-C Cable and Connector Specification Revision 1.3
– Compliant to USB Power Delivery Specification Revision 3.0 Version 1.1
– Integrated Type-C transceivers, supporting one charging UFP and up to two DRP DFPs
– Built-in pull-up/pull down resistors, including Rp, Rd, and Ra
– Built-in Vconn power switch

■**DP Alt-mode Configuration**
– Compliant to VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0a
– DP mode Discovery/Enter/Exit; DP configure, status update, source/sink connection detection
– Built-in Aux_CH switch

■**USB-C Charging UFP Capability**
– Charging connected PD hosts once external power is available
– Support Provider and Consumer roles
– Support PD Power Rule up to 100W
– Support dead battery charging and PD3.0 Fast Role Swap

■**Two USB-C DRP DFPs Capability**
– Support Provider and Consumer roles
– Support PD Power Rule up to 100W as Sink and 15W as Source
– Either DFP port can charge host (as sink) by first-plugin-first-serve basis, the other port is then set to source mode only

■**USB Interface and USB Billboard Device**
– USB Billboard compliant to USB Device Class Definition for Billboard Devices Revision 1.21
– Integrated in-house USB2.0 Full-speed PHY
– Proprietary design for interchangeable charge through audio to select USB routing by first-plugin-first-serve basis

■**Fast 8051 Macro Cell 80C32-Compatible Microcontroller**
– Standard 1T 8051 instruction set with embedded Mask ROM and SRAM
– Support external SPI flash or sharing SPI flash with VLI Hub controller for firmware upgrade

■**HV Process and Built-in Buck Controller, Oscillator, Voltage Regulators, Voltage and Current Detectors**
– Adopting HV process; CC pins and SBU pins can tolerate up to 22V
– Built-in 20V-to-5V DC-to-DC buck controller with bypass mode for powering system and Hub DFPs
– Built-in trimmed RC oscillator
– Built-in 5V-to-3.3V LDO and 3.3V-to-1.8V LDO
– Built-in 20V-to-5V LDO for charge through audio applications
– Vbus Voltage Detector and Vbus Current Detector for monitoring power safety

■**Smart Auto-standby**
– Automatically entering deep power saving mode when connected interface is in idle state

■**GPIOs for Special Function and Control**
– 10 GPIOs in QFN60/VFBGA69 and 8 GPIOs in QFN48 for application customization and one I^2C master interface

■**Physical**
– QFN 60 green package (7x7x0.85 mm) for VL104-Q6
– QFN 48 green package (6x6x0.85 mm) for VL104-Q4
– VFBGA 69 green package (5x5x0.87 mm) for VL104FA with on-chip SPI flash

■**Certification**
– TBD

■**Applications**
– USB-C charge through dongle or Multi-function dongle with any port charge through
– USB-C interchangeable charge through audio dongle

VL104 System Overview

VIA Lab's VL104 is a highly integrated single chip DisplayPort Alt-mode and Power Delivery 3.0 controller for USB-C devices designed for USB-C multi-function docks with charge through and interchangeable charge through audio dongles. Integrated USB-C charging UFP, VL104 can perform DP alt-mode video output functionality and simultaneously charging connected PD host once external power is detected. Two integrated USB-C DRP DFPs can either connect to USB-C power adapter to charge PD host or connect to USB-C devices to access data transfer. Either DFP port can charge host by first-plugin-first-serve basis. VL104's Device Policy Manager could negotiate power rules between its DFP and UFP then enable power charge through. Charging a host under dead battery mode and PD3.0 fast role swap are supported. A proprietary design for USB D+/D- routing is implemented by first-plugin-first-serve basis to support interchangeable charge through audio. SBU1/SBU2 switch is built-in to support USB-C cable flipping feature. USB Billboard device function is included to meet "VESA DP Alt-Mode on USB Type-C" spec. VL104 also support smart auto-standby that automatically entering deep power saving mode when connected interface is in idle state which is suitable for smart phone accessories.

Adopting HV process, 20V to 5V Buck controller is built-in to save BOM and CC pins and SBU pins can tolerate to 22V. Built-in trimmed RC oscillator, linear voltage regulators, Vbus voltage and current detectors, VL104 can work perfectly without external buck-boost circuitry and monitor abnormal power behavior. Up to 10 GPIO pins are available for specific application usage. The SPI interface can support external SPI flash or sharing SPI flash with VLI Hub controller for firmware upgrade. VL104 is available in QFN 60L (7x7x0.85 mm) that supports two DRP DFPs and QFN 48L (6x6x0.85 mm) that supports one DRP DFP. VFBGA 69L (5x5x0.87 mm) with on-chip SPI flash is also available to meet PCB space-constraint design.

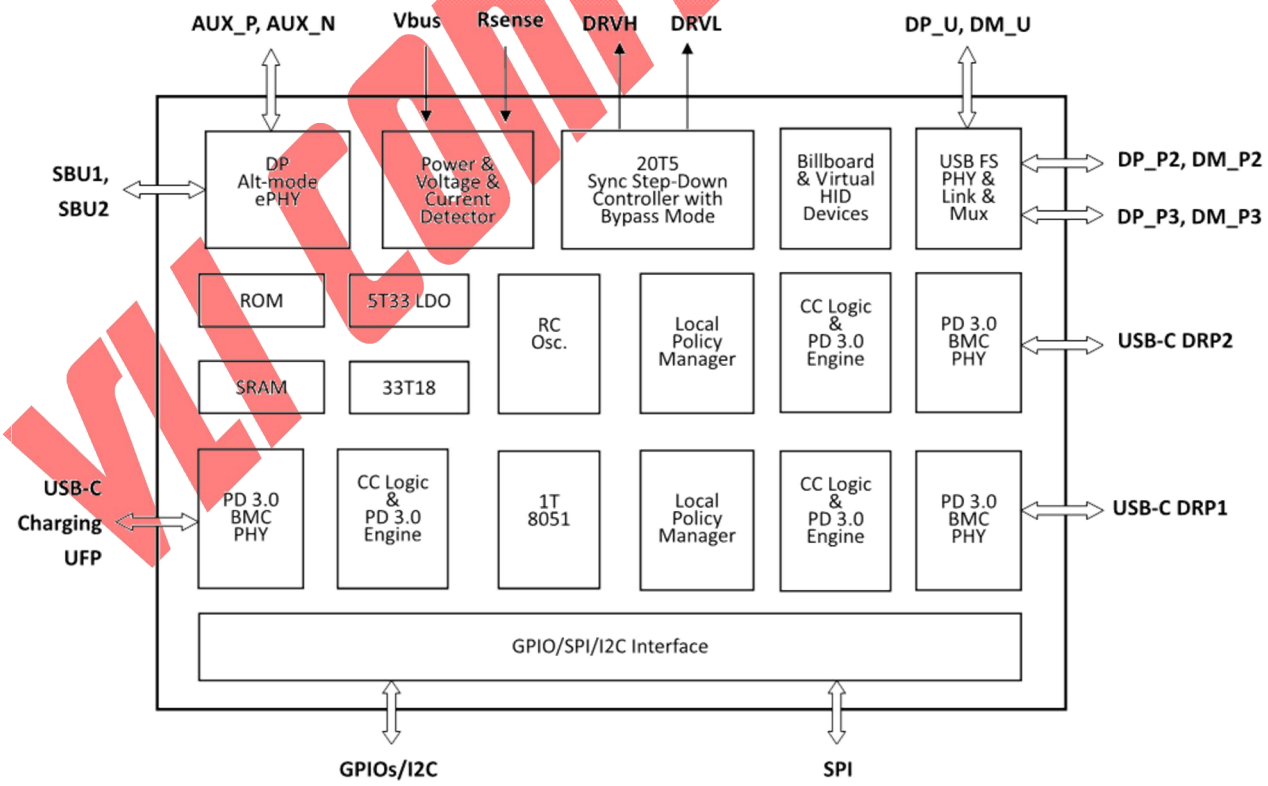


Figure 1 – VL104 Block Diagram

Typical Applications

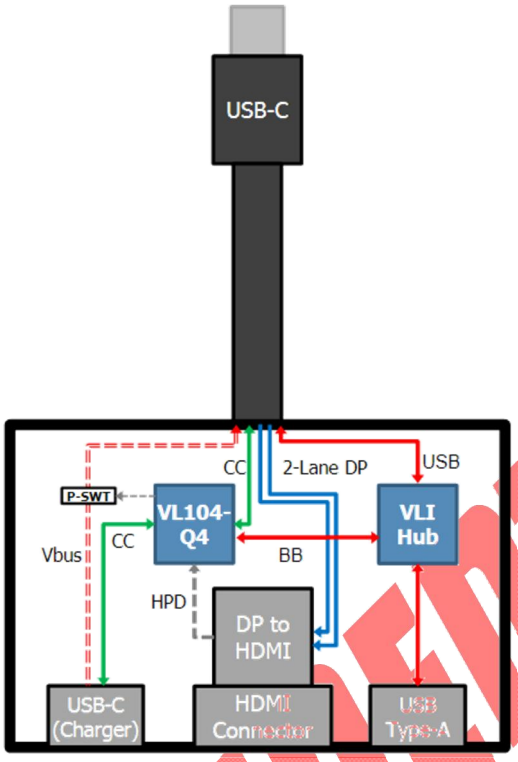


Figure 2 – Generic VL104-Q4 USB-C Multi-function Charge Through Dongle

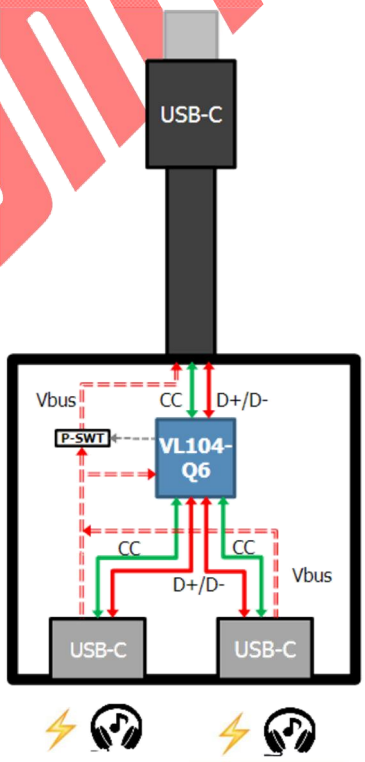


Figure 3 – VL104-Q6 USB-C Interchangeable Charge Through Audio Dongle

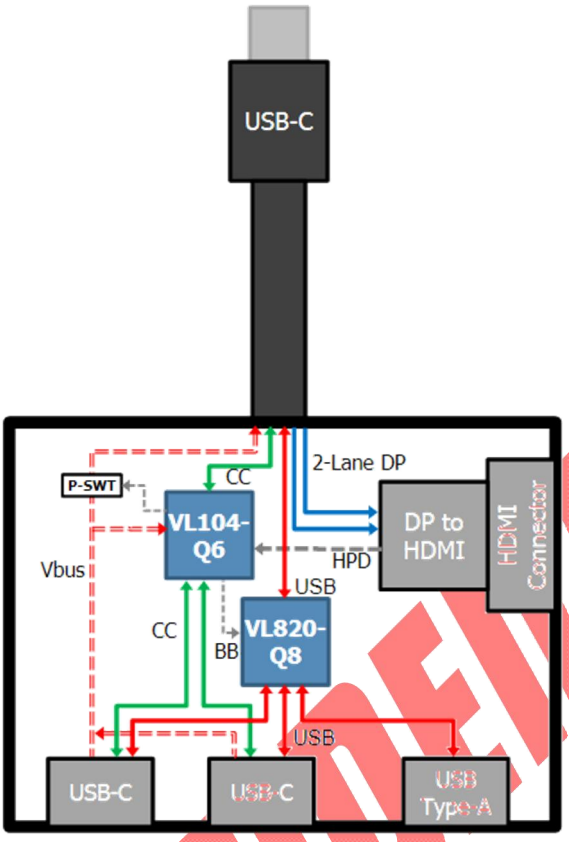


Figure 4 – Generic VL104-Q6 USB-C Multi-function Dongle with Any Port Charge Through

Pinout

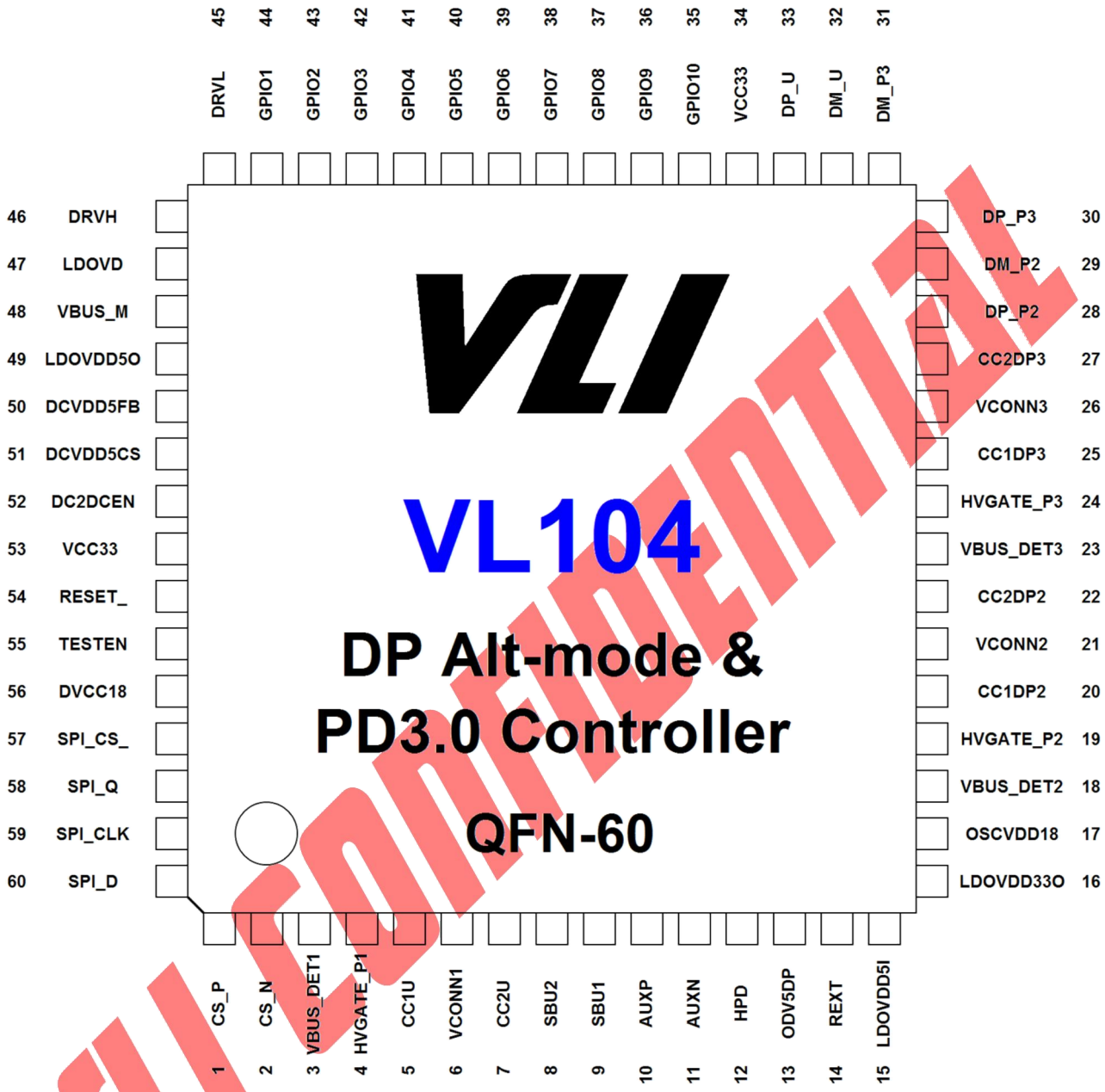


Figure 5 – VL104 QFN-60 Pin Diagram

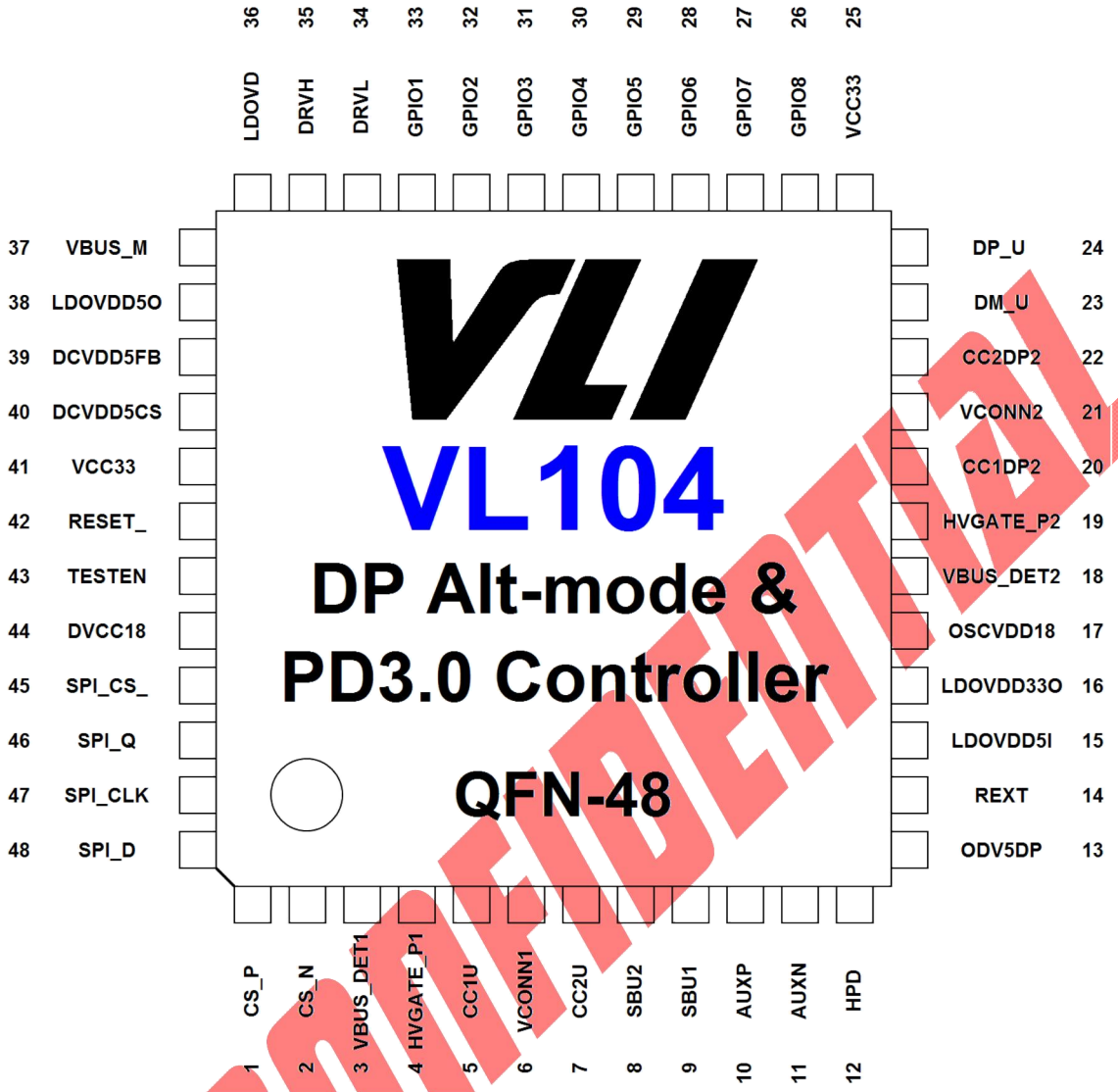


Figure 6 – VL104 QFN-48 Pin Diagram

	1	2	3	4	5	6	7	8	9	
A	VSS	VBUS_M	LDOVD	GPIO4	GPIO7	DM_U	DP_P3	DP_P2	VSS	A
B	LDOVDD5O	DRVH	DRVL	GPIO3	GPIO6	DP_U	DM_P3	DM_P2	CC2DP3	B
C	DCVDD5FB	DCVDD5CS	GPIO1	GPIO2	GPIO5	GPIO8	GPIO10	HVGATE_P3	VCONN3	C
D	DC2DC_EN	RESET_					GPIO9	VBUS_DET3	CC1DP3	D
E	DVCC18	TESTEN		VDD5V	VCC33			VCONN2	CC2DP2	E
F	SPI_CS_	SPI_Q		VSS	VSS			HVGATE_P2	CC1DP2	F
G	SPI_CLK	SPI_D		VSS	VSS		ODV5DP	VBUS_DET2	OSCVDD18	G
H	CS_N	VBUS_DET1	HVGATE_P1	VSS	SBU1	AUXP	HPD	REXT	LDOVDD33O	H
J	VSS	CS_P	CC1U	VCONN1	CC2U	SBU2	AUXN	LDOVDD5I	VSS	J
	1	2	3	4	5	6	7	8	9	

Figure 7 – VL104 VFBGA-69 Pin Diagram

Pin List

Table 1 – VL104 QFN-60 Pin List

Pin	Pin Name	Pin	Pin Name
1	CS_P	31	DM_P3
2	CS_N	32	DM_U
3	VBUS_DET1	33	DP_U
4	HVGATE_P1	34	VCC33
5	CC1U	35	GPIO10
6	VCONN1	36	GPIO9
7	CC2U	37	GPIO8
8	SBU2	38	GPIO7
9	SBU1	39	GPIO6
10	AUXP	40	GPIO5
11	AUXN	41	GPIO4
12	HPD	42	GPIO3
13	ODV5DP	43	GPIO2
14	REXT	44	GPIO1
15	LDOVDD5I	45	DRVL
16	LDOVDD33O	46	DRVH
17	OSCVDD18	47	LDOVD
18	VBUS_DET2	48	VBUS_M
19	HVGATE_P2	49	LDOVDD5O
20	CC1DP2	50	DCVDD5FB
21	VCONN2	51	DCVDD5CS
22	CC2DP2	52	DC2DCEN
23	VBUS_DET3	53	VCC33
24	HVGATE_P3	54	RESET_
25	CC1DP3	55	TESTEN
26	VCONN3	56	DVCC18
27	CC2DP3	57	SPI_CS_
28	DP_P2	58	SPI_Q
29	DM_P2	59	SPI_CLK
30	DP_P3	60	SPI_D

Table 2 – VL104 QFN-48 Pin List

Pin	Pin Name	Pin	Pin Name
1	CS_P	25	VCC33
2	CS_N	26	GPIO8
3	VBUS_DET1	27	GPIO7
4	HVGATE_P1	28	GPIO6
5	CC1U	29	GPIO5
6	VCONN1	30	GPIO4
7	CC2U	31	GPIO3
8	SBU2	32	GPIO2
9	SBU1	33	GPIO1
10	AUXP	34	DRVL
11	AUXN	35	DRVH
12	HPD	36	LDOVD

13	ODV5DP	37	VBUS_M
14	REXT	38	LDOVDD5O
15	LDOVDD5I	39	DCVDD5FB
16	LDOVDD33O	40	DCVDD5CS
17	OSCVDD18	41	VCC33
18	VBUS_DET2	42	RESET_
19	HVGATE_P2	43	TESTEN
20	CC1DP2	44	DVCC18
21	VCONN2	45	SPI_CS_
22	CC2DP2	46	SPI_Q
23	DM_U	47	SPI_CLK
24	DP_U	48	SPI_D

Table 3 – VL104 VFBGA-69 Pin List

Pin	Pin Name	Pin	Pin Name
A1	VSS	E5	VCC33
A2	VBUS_M	E8	VCONN2
A3	LDOVD	E9	CC2DP2
A4	GPIO4	F1	SPI_CS_
A5	GPIO7	F2	SPI_Q
A6	DM_U	F4	VSS
A7	DP_P3	F5	VSS
A8	DP_P2	F8	HVGATE_P2
A9	VSS	F9	CC1DP2
B1	LDOVDD5O	G1	SPI_CLK
B2	DRVH	G2	SPI_D
B3	DRVL	G4	VSS
B4	GPIO3	G5	VSS
B5	GPIO6	G7	ODV5DP
B6	DP_U	G8	VBUS_DET2
B7	DM_P3	G9	OSCVDD18
B8	DM_P2	H1	CS_N
B9	CC2DP3	H2	VBUS_DET1
C1	DCVDD5FB	H3	HVGATE_P1
C2	DCVDD5CS	H4	VSS
C3	GPIO1	H5	SBU1
C4	GPIO2	H6	AUXP
C5	GPIO5	H7	HPD
C6	GPIO8	H8	REXT
C7	GPIO10	H9	LDOVDD33O
C8	HVGATE_P3	J1	VSS
C9	VCONN3	J2	CS_P
D1	DC2DCEN	J3	CC1U
D2	RESET_	J4	VCONN1
D7	GPIO9	J5	CC2U
D8	VBUS_DET3	J6	SBU2
D9	CC1DP3	J7	AUXN
E1	DVCC18	J8	LDOVDD5I
E2	TESTEN	J9	VSS
E4	VDD5V		

Pin Descriptions

Signal Type Definition

Name	Type	Signal Description
Input	I	A standard input-only signal
Output	O	A standard active driver
Input/ Output	I/O	A bi-directional signal
Analog bias	A_{BIAS}	Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network
Power	PWR	A power pin
Ground	GND	A ground pin

USB-C Interface

Pin Name	QFN60	QFN48	VFBGA69	I/O	Signal Description
CC1U	5	5	J3	I/O	Charging UFP Configuration Channel 1
CC2U	7	7	J5	I/O	Charging UFP Configuration Channel 2
CC1DP2	20	20	F9	I/O	DRP DFP Port2 Configuration Channel 1
CC2DP2	22	22	E9	I/O	DRP DFP Port2 Configuration Channel 2
CC1DP3	25	—	D9	I/O	DRP DFP Port3 Configuration Channel 1
CC2DP3	27	—	B9	I/O	DRP DFP Port3 Configuration Channel 2
SBU1	9	9	H5	I/O	Sideband Use 1
SBU2	8	8	J6	I/O	Sideband Use 2

USB Interface & USB Billboard

Pin Name	QFN60	QFN48	VFBGA69	I/O	Signal Description
DP_U	33	24	B6	I/O	D+ Data Line to USB Billboard Device or Audio Input
DM_U	32	23	A6	I/O	D– Data Line to USB Billboard Device or Audio Input
DP_P2	28	—	A8	I/O	D+ Data Line Connect to DFP Port2 for USB Audio
DM_P2	29	—	B8	I/O	D– Data Line Connect to DFP Port2 for USB Audio
DP_P3	30	—	A7	I/O	D+ Data Line Connect to DFP Port3 for USB Audio
DM_P3	31	—	B7	I/O	D– Data Line Connect to DFP Port3 for USB Audio

DP Alt-mode Interface

Pin Name	QFN60	QFN48	VFBGA69	I/O	Signal Description
AUXP	10	10	H6	I/O	DP AUX Channel Positive
AUXN	11	11	J7	I/O	DP AUX Channel Negative
HPD	12	12	H7	I	DP Hot Plug Detect

SPI Interface

Pin Name	QFN60	QFN48	VFBGA69	I/O	Signal Description
SPI_CS_	57	45	F1	O	Serial Flash Chip Enable
SPI_D	60	48	G2	O	Serial Flash Data Input
SPI_Q	58	46	F2	I	Serial Flash Data Output
SPI_CLK	59	47	G1	O	Serial Flash Clock

Analog Command Block

Pin Name	QFN60	QFN48	VFBGA69	I/O	Signal Description
REXT	14	14	H8	A_{BIAS}	Connect to External Resistor (243K ohm, +/- 1% accuracy)
VBUS_M	48	37	A2	PWR	5V~20V Power Input for VL104
DRVH	46	35	B2	O	High Side MOSFET Gate Driver
DRVL	45	34	B3	O	Low Side MOSFET Gate Driver
DCVDD5FB	50	39	C1	O	5V Feedback Pin
DCVDD5CS	51	40	C2	I	5V Current Sense Pin
HVGATE_P1	4	4	H3	O	Charge Pump Output for Charging UFP
HVGATE_P2	19	19	F8	O	Charge Pump Output for DRP DFP Port2
HVGATE_P3	24	—	C8	O	Charge Pump Output for DRP DFP Port3
LDOVDD5O	49	38	B1	PWR	20V to 5V LDO Power Output
LDOVDD5I	15	15	J8	PWR	5V to 3.3V LDO Power Input
LDOVDD33O	16	16	H9	PWR	3.3V Output Loading Capacitor Pin for 5V to 3.3V LDO
OSCVDD18	17	17	G9	PWR	OSC 1.8V Power Input
LDOVD	47	36	A3	O	High Side Driver for LDO Power Output Sync
VCONN1	6	6	J4	PWR	5V Input Power for Charging UFP VCONN
VCONN2	21	21	E8	PWR	5V Input Power for DRP DFP Port2 VCONN
VCONN3	26	—	C9	PWR	5V Input Power for DRP DFP Port3 VCONN
VBUS_DET1	3	3	H2	I	Charging UFP VBus Power Input for Removal Detection
VBUS_DET2	18	18	G8	I	DRP DFP Port2 Vbus Power Input for Removal Detection
VBUS_DET3	23	—	D8	I	DRP DFP Port3 Vbus Power Input for Removal Detection
CS_P	1	1	J2	I	Current Sensing Positive Input
CS_N	2	2	H1	I	Current Sensing Negative Input
ODV5DP	13	13	G7	O	Open-Drain Output for 5V Video Power Control
DC2DCEN	52	—	D1	I	DC-to-DC Regulator Enable Control

General Purpose I/O and Miscellaneous

Pin Name	QFN60	QFN48	VFBGA69	I/O	Signal Description
RESET_	54	42	D2	I	External Chip Reset
GPIO1	44	33	C3	I/O	General Purpose I/O
GPIO2	43	32	C4	I/O	General Purpose I/O
GPIO3	42	31	B4	I/O	General Purpose I/O
GPIO4	41	30	A4	I/O	General Purpose I/O
GPIO5	40	29	C5	I/O	General Purpose I/O
GPIO6	39	28	B5	I/O	General Purpose I/O
GPIO7	38	27	A5	I/O	General Purpose I/O
GPIO8	37	26	C6	I/O	General Purpose I/O
GPIO9	36	—	D7	I/O	General Purpose I/O
GPIO10	35	—	C7	I/O	General Purpose I/O

Test Pin

Pin Name	QFN60	QFN48	VFBGA69	I/O	Signal Description
TESTEN	55	43	E2	I	Test Mode Enable; Internal pull down Do not connect for normal operation.

Power and Ground

Pin Name	QFN60	QFN48	VFBGA69	I/O	Signal Description
VDD5V	—	—	E4	PWR	E-fuse Power Input, Connecting to 3.3V in Normal Use
VCC33	34, 53	25, 41	E5	PWR	3.3V Digital IO Power
DVCC18	56	44	E1	PWR	1.8V Core Power
VSS	EPAD	EPAD	A1, A9, F4, F5, G4, G5, H4, J1, J9	GND	Ground

Electrical Specification

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-55	125	°C	—
V_{BUS_MAX}	V_{BUS} Supply Voltage	—	22	V	Absolute Max
V_{DD33}	3.3V Power Input Voltage	-0.5	3.69	V	—
V_{DD50}	5V Power Input Voltage	-0.5	5.5	V	—
V_O	Output Voltage at any output	-0.5	VCC+ 0.5	V	—
V_{ESD}	Electrostatic Discharge	-2	2	kV	Human Body Model
Θ_{JC}	Thermal resistance between junction and case	QFN48 for 4-layer PCB: 12.8 QFN60 for 4-layer PCB: 13.3 BGA69 for 4-layer PCB: 18.8		°C/W	4L PCB definitions follow JESD51-7
Θ_{JA}	Thermal resistance between junction and ambient	QFN48 for 4-layer PCB: 28.6 QFN60 for 4-layer PCB: 28 BGA69 for 4-layer PCB: 51.9		°C/W	
P_D	Max Power Dissipation	—	TBD	mW	—

Note:
1. Stress above conditions may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described.
2. About thermal factors, T_A is the concerned ambient temperature, and
   $\Theta_{CA} = \theta_{JA} - \theta_{JC}$
   $T_J = \theta_{JA} * P_D + T_A$
   $T_C = \theta_{CA} * P_D + T_A$

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VBUS_M	VL104 Power Input	4.5		22	V
LDOVDD5I	5V to 3.3V LDO 5V Power Input	4.5	5	5.5	V
VCC33	Digital IO power 3.3V	3.0	3.3	3.6	V
DVCC18	Digital Core power 1.8V	1.62	1.8	1.98	V
DGND	Ground	—	0	—	V
T_A	Ambient Temperature	0		70	°C
T_J	Junction Temperature	0		125	°C

General IO DC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.30	0.8	V	—
V_{IH}	Input High Voltage	2.0	3.6	V	—
V_{OL}	Output Low Voltage	—	0.4	V	IOL=15.8mA
V_{OH}	Output High Voltage	2.4	—	V	IOH=26.5mA
I_{IL}	Input Leakage Current	—	+/-10	µA	0<VIN<VCC
I_{OZ}	Tristate Leakage Current	—	+/-10	µA	0<VOUT<VCC

Internal 20V to 5V DC-to-DC Buck Controller

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	4.5		22	V	
Output Voltage	4.5	5	5.25	V	
Feedback Voltage	4.5	5	5.5	V	
Current Sense Voltage	4.5	5	5.5	V	
Max. Output Current			6	A	

Internal 3.3V to 1.8V LDO Regulator

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	3.0	3.3	3.6	V	
Output Voltage	1.71	1.8	1.89	V	
Max. Output Current			100	mA	

Internal 5V to 3.3V LDO Regulator

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	4.5	5.0	5.5	V	
Output Voltage	3.135	3.3	3.465	V	
Max. Output Current			100	mA	

PD BMC DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
$V_{BMCSWING}$	Voltage Swing	1.05	1.2	V	—
Z_{BMCDRV}	Drive Output Resistance	33	75	Ω	—
T_{BMCR}	Rise Time	300		ns	—
T_{BMCF}	Fall Time	300		ns	—

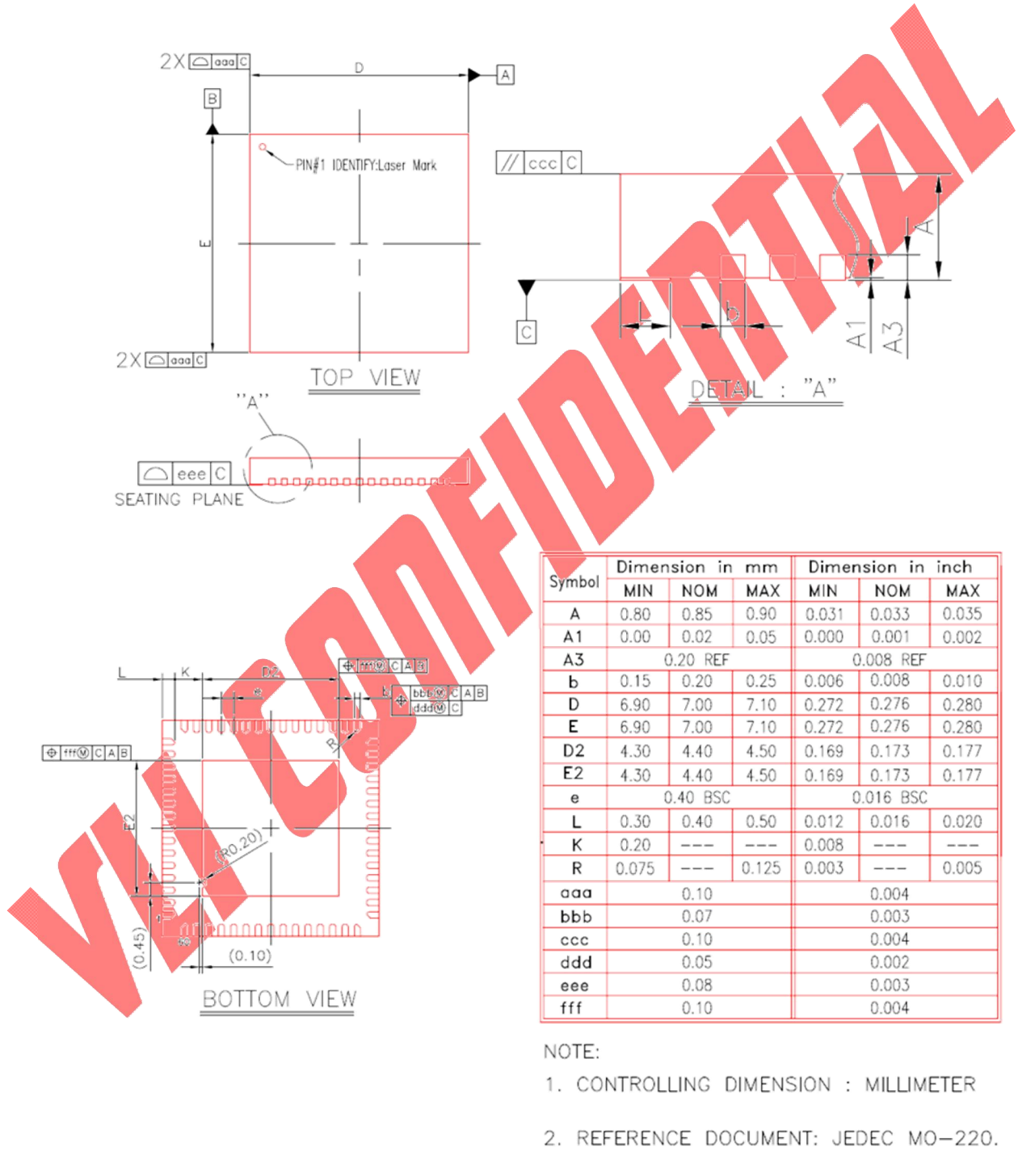
USB Full Speed DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{IH}	High state input level	2.0		V	—
V_{IHZ}	High-z state input level	2.7	3.6	V	—
V_{IL}	Low state input level		0.8	V	—
V_{DI}	Differential input sensitivity	0.2		V	—
V_{CM}	Differential common mode	0.8	2.5	V	—
V_{OL}	Low state output level	0.0	0.3	V	—
V_{OH}	High state output level	2.8	3.6	V	—
V_{CRS}	Output signal crossover voltage	1.3	2.0	V	—
R_{PU}	Bus pull-up resistor	1.425	1.575	KΩ	—
Z_{DRV}	Driver output resistance	28	44	Ω	—
T_{FR}	Full-speed Rise Time	4	20	ns	—
T_{FF}	Full-speed Fall Time	4	20	ns	—

Package Mechanical Specifications

QFN-60 Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	250	°C
Max Time within 5°C of Tp	30	seconds



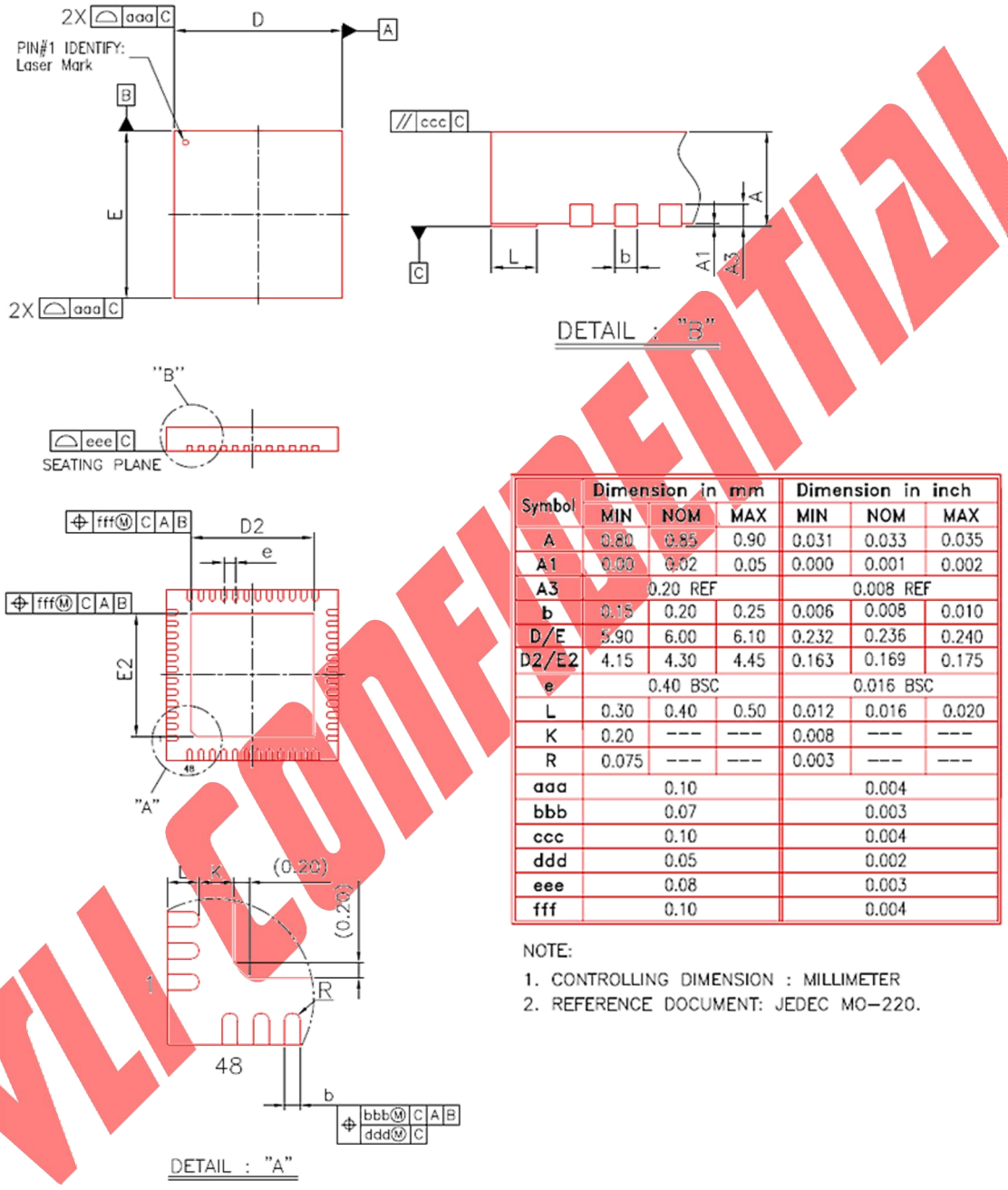
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.90	7.00	7.10	0.272	0.276	0.280
E	6.90	7.00	7.10	0.272	0.276	0.280
D2	4.30	4.40	4.50	0.169	0.173	0.177
E2	4.30	4.40	4.50	0.169	0.173	0.177
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	0.125	0.003	---	0.005
aaa		0.10			0.004	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	
fff		0.10			0.004	

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 8 – QFN 60L 7x7x0.85 mm Mechanical Specification

QFN-48 Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	250	°C
Max Time within 5°C of Tp	30	seconds



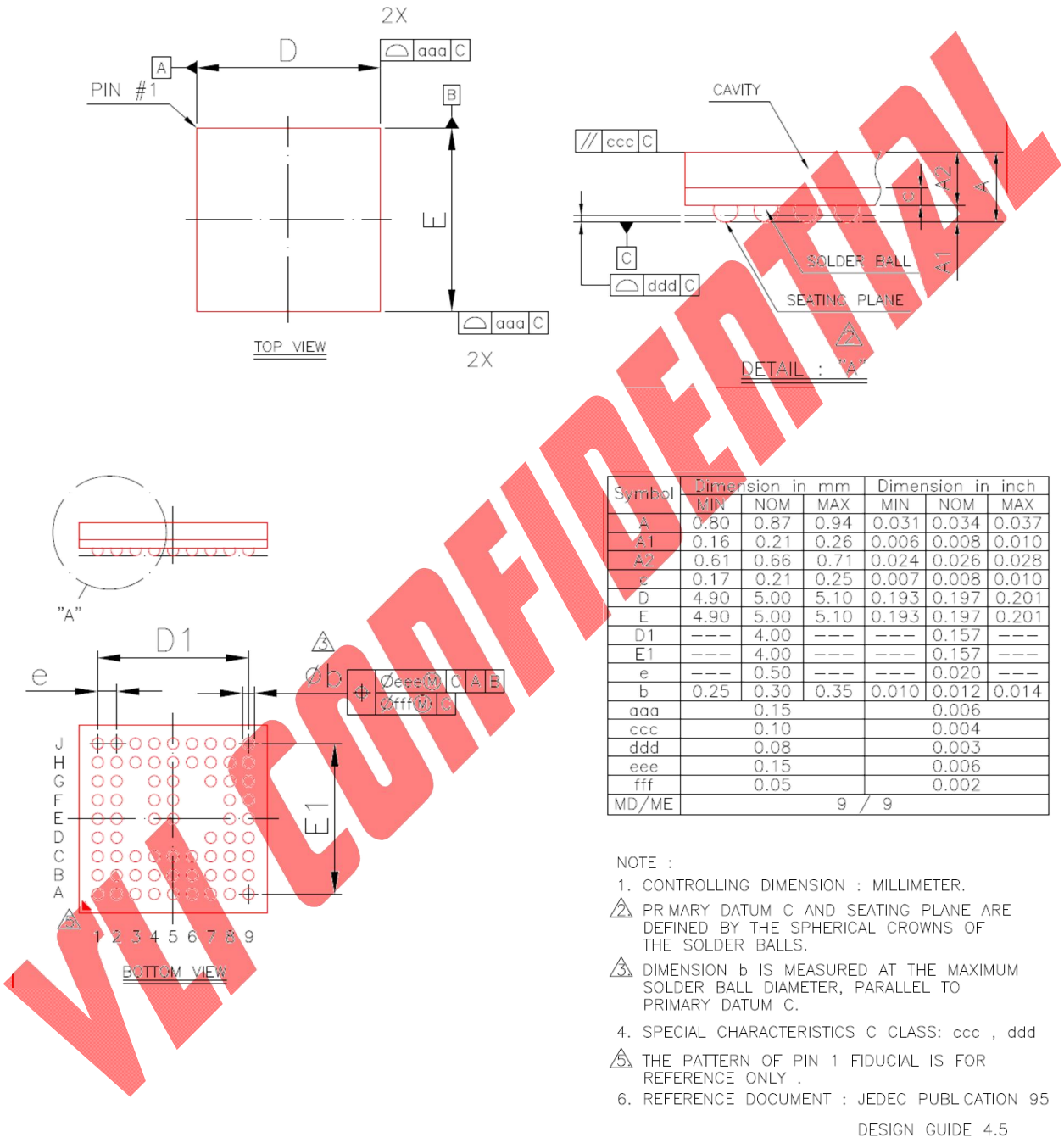
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
D2/E2	4.15	4.30	4.45	0.163	0.169	0.175
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa		0.10			0.004	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	
fff		0.10			0.004	

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 9 – QFN 48L 6x6x0.85 mm Mechanical Specification

VFBGA-69 Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	260	°C
Max Time within 5°C of Tp	30	Seconds



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.87	0.94	0.031	0.034	0.037
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.61	0.66	0.71	0.024	0.026	0.028
c	0.17	0.21	0.25	0.007	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
E	4.90	5.00	5.10	0.193	0.197	0.201
D1	---	4.00	---	---	0.157	---
E1	---	4.00	---	---	0.157	---
e	---	0.50	---	---	0.020	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa		0.15			0.006	
ccc		0.10			0.004	
ddd		0.08			0.003	
eee		0.15			0.006	
fff		0.05			0.002	
MD/ME		9 / 9				

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: ccc , ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .
6. REFERENCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5

Figure 10 – VFBGA 69L 5x5x0.87 mm Mechanical Specification

Package Top Side Marking

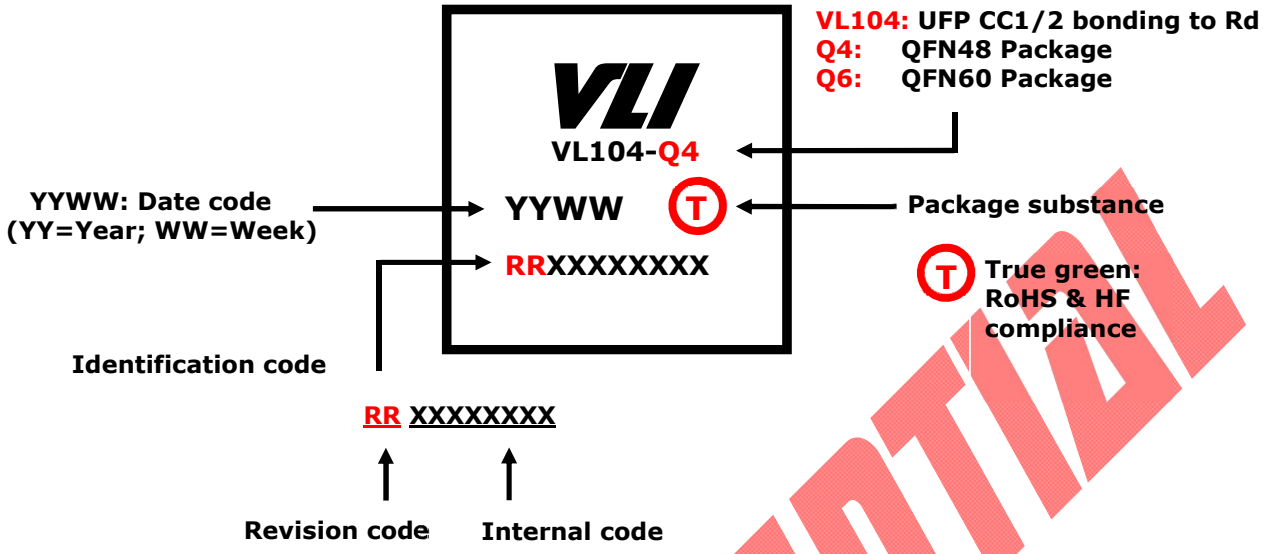


Figure 11 – VL104 QFN Package Top Side Marking

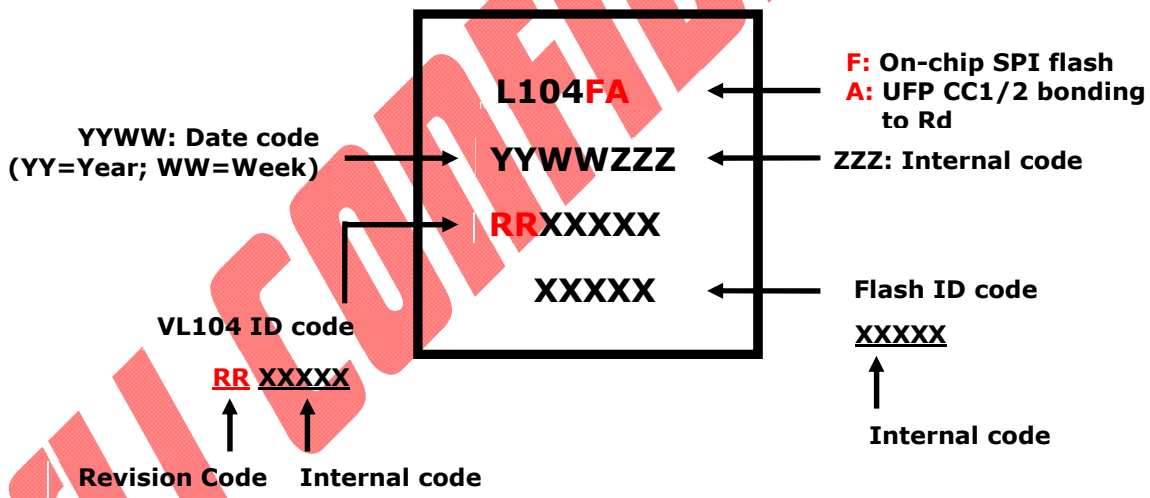


Figure 12 – VL104 VFBGA Package Top Side Marking

Ordering Information

Please contact VIA Labs sales representative or distributor in your region for ordering part number details.

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