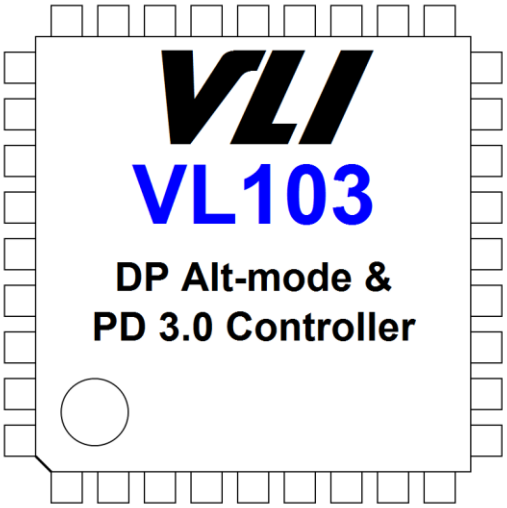
VIA Labs, Inc.

Datasheet

VL103
DP Alt-mode & PD 3.0 Controller with Auto-Standby for USB-C Devices

February 23rd, 2018

Revision 1.00



Revision History

Rev	Date	Note	Initial
0.80	08/04/2017	Preliminary release	HC
1.00	02/23/2018	Modify REXT value Update USB Billboard to Revision 1.21 Update top side marking rules Add USB-IF PD2.0 Certification TID Add VFBGA pin list, package, and top marking information Add thermal resistance data Remove ordering information	HC

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Product Features

VL103

DisplayPort Alt-mode & PD 3.0 Controller with Auto-Standby for USB-C Devices

■CC Logic & PD 3.0 Engine supporting one charging UFP and one DRP
– Compliant to USB Type-C Cable and Connector Specification Revision 1.2
– Compliant to USB Power Delivery Specification Revision 3.0 Version 1.0a
– Integrated Type-C transceivers, supporting one charging UFP and one DRP
– Built-in pull-up/pull down resistors, including Rp, Rd, and Ra
– Built-in Vconn power switch

■DP Alt-mode Configuration
– Compliant to VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0a
– DP mode Discovery/Enter/Exit
– DP configure, status update, source/sink connection detection
– Built-in Aux_CH switch

■USB-C Charging UFP Capability
– Charging connected PD hosts once external power is available
– Support Provider and Consumer roles
– Support PD Power Rule up to 100W
– Support dead battery charging and Fast Role Swap

■USB-C DRP Capability
– Support Provider and Consumer roles
– Support PD Power Rule up to 100W as Sink and 15W as Source
– Built-in D+/D- Charging ePHY for chargers using D+/D- as protocol handshake
– Built-in USB HS data switch

■USB Billboard Device
– Compliant to USB Device Class Definition for Billboard Devices Revision 1.21
– Integrated in-house USB2.0 Full-speed PHY

■Fast 8051 Macro cell 80C32-Compatible Microcontroller
– Standard 1T 8051 instruction set
– Embedded Mask ROM and SRAM
– Support external SPI flash or sharing SPI flash with VLI Hub controller for firmware upgrade

■Built-in Oscillator, Voltage Regulators, Voltage Detector, and Current Detector
– Built-in trimmed RC oscillator
– 5.0V-to-3.3V LDO and 3.3V-to-1.8V LDO
– Auto power source selection between Vbus and Vconn
– Vbus Voltage Detector and Vbus Current Detector for monitoring power safety

■Smart Auto-standby
– Automatically entering deep power saving mode when connected interface is in idle state

■GPIOs for Special Function and Control
– 11 GPIOs in QFN48/VFBGA45 and 7 GPIOs in QFN32 for application customization and one I^2C master interface

■Physical
– QFN 48 green package (6x6x0.85 mm) for VL103-Q4, VL103R-Q4, and VL103S-Q4; pin-to-pin compatible to VL102-Q4
– QFN 32 green package (5x5x0.85 mm) for VL103-Q3; pin-to-pin compatible to VL100-Q3
– VFBGA 45 green package (4x4x0.87 mm) for VL103FA with on-chip SPI flash

■Certification
– VL103-Q3 PD 2.0 Certification TID: 1060047; VL103-Q4 PD 2.0 Certification TID: 1060043

■Applications
– USB-C video adapters
– USB-C Multi-function docks

VL103 System Overview

VIA Lab's VL103 is a highly integrated power-saving single chip DisplayPort Alt-mode and Power Delivery 3.0 controller for USB-C devices that designed for applications like USB-C video adapters and USB-C multi-function docking stations. Integrated USB-C charging UFP, VL103 can perform DP alt-mode video output functionality and simultaneously charging connected PD host once external power is detected. Integrated second USB-C DRP can either connect to USB-C power adapter to charge PD host or connect to USB-C devices to access data transfer. A D+/D- charging ePHY is integrated to support chargers using D+/D- pins to do protocol handshake. VL103's Device Policy Manager could negotiate power rules between its DRP and UFP then enable power charging-through. Charging a host under dead battery mode and PD3.0 fast role swap are supported. SBU1/SBU2 switch is built-in to support USB-C cable flipping feature. USB Billboard device function is implemented to meet "VESA DP Alt-Mode on USB Type-C" spec. VL103 also support smart auto-standby that automatically entering deep power saving mode when connected interface are in idle state which is suitable for smart phone accessories.

Built-in trimmed RC oscillator, linear voltage regulators, Vbus voltage detector, and Vbus current detector, VL103 can work perfectly with power input either from Vconn power or from Vbus power and can monitor abnormal power behavior. Up to 11 GPIO pins are available for power discharge control, power switch control, data switch control, or other special application usage. The SPI interface can support external SPI flash or sharing SPI flash with VLI Hub controller for firmware upgrade. VL103 is available in QFN 48L (6x6x0.85 mm) that pin-to-pin compatible to VL102-Q4 and QFN 32L (5x5x0.85 mm) that pin-to-pin compatible to VL100-Q3. VFBGA 45L (4x4x0.87 mm) with on-chip SPI flash is also available to meet PCB space-constraint design.

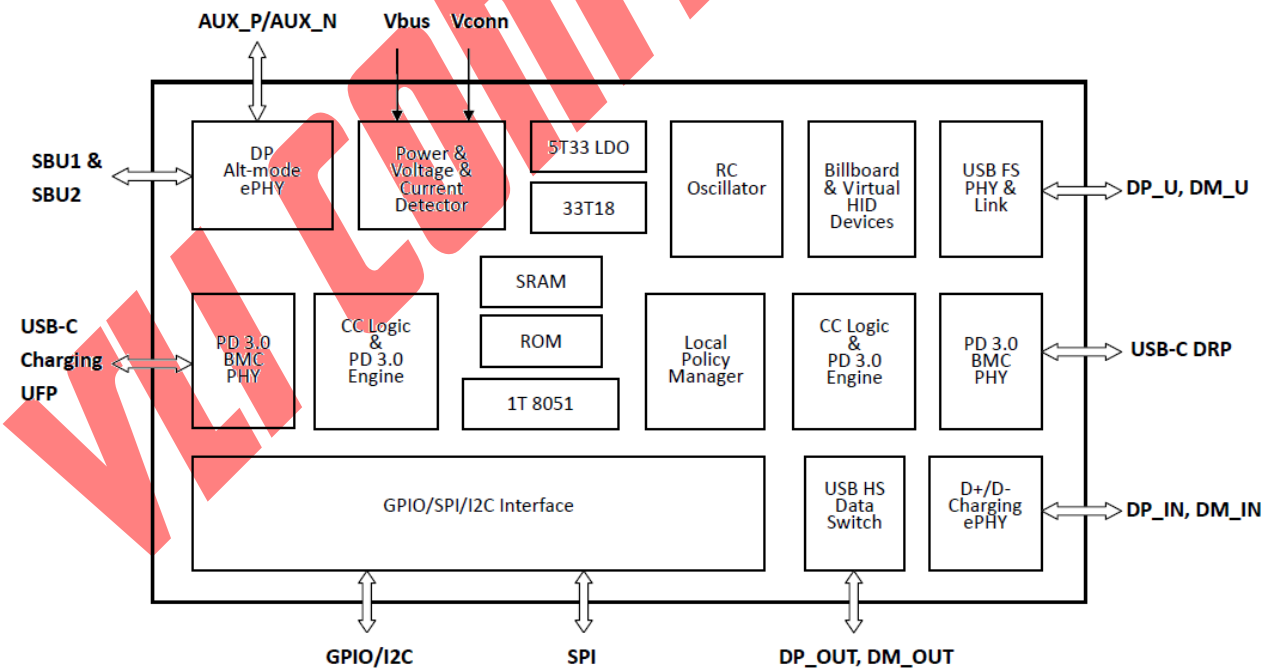


Figure 1 – VL103 Block Diagram

Typical Applications

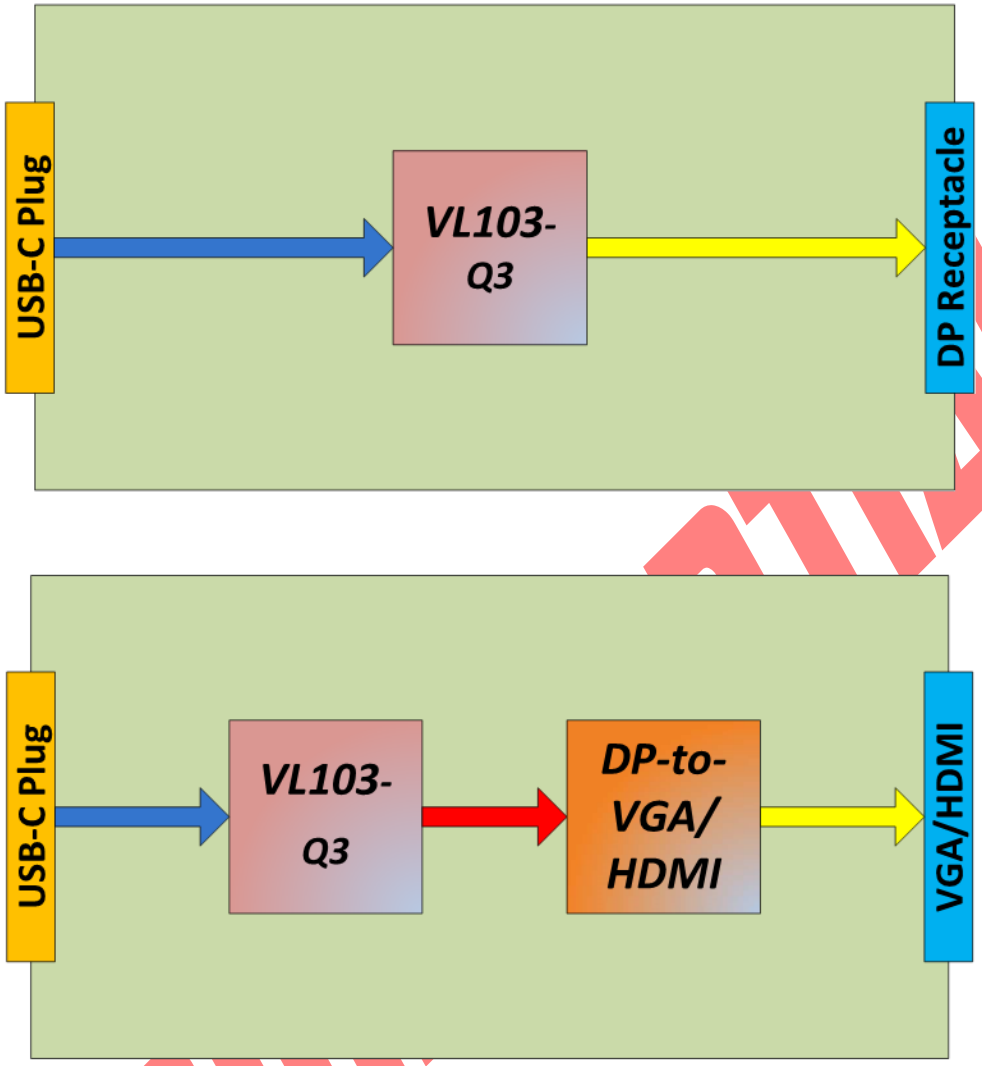


Figure 2 – Generic VL103 USB-C Video Adapters

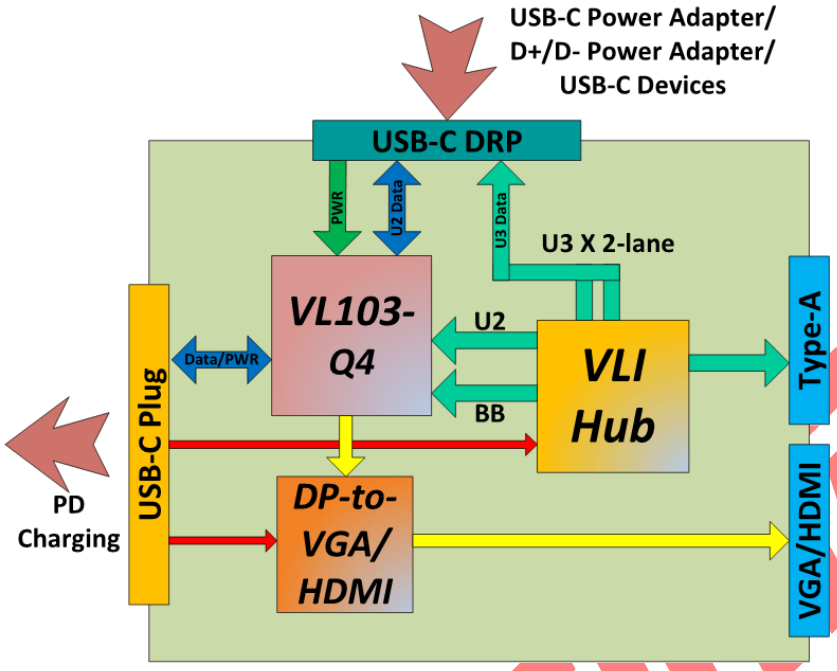


Figure 3 – VL103 USB-C Video Adapters with Hub and PD Charging-Thru

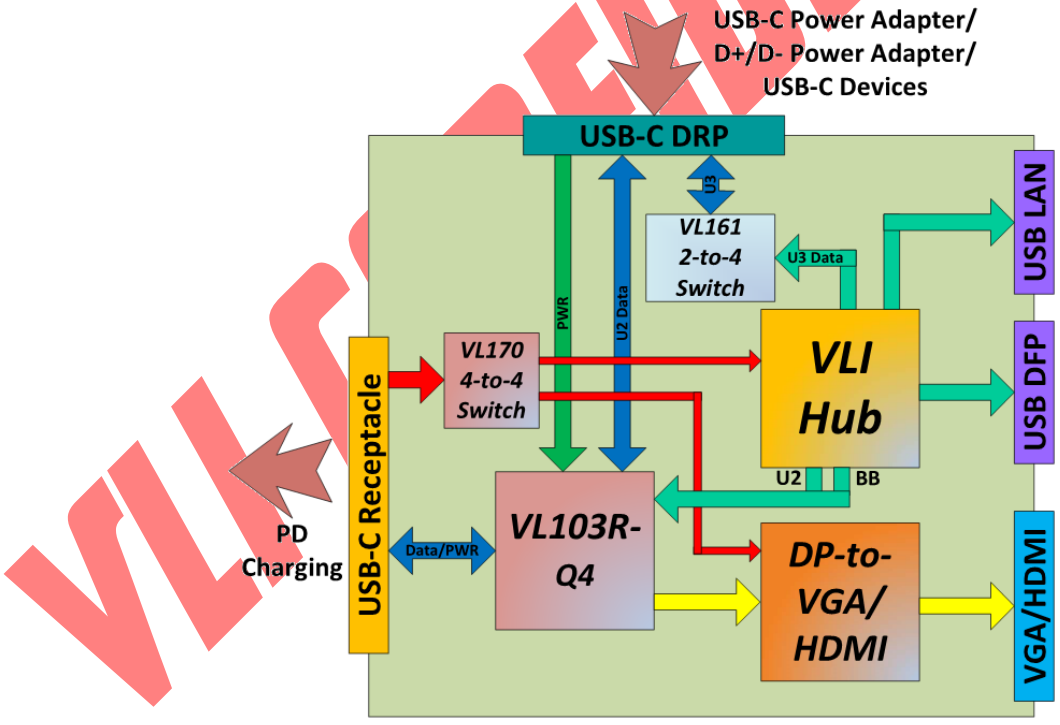


Figure 4 – VL103R USB-C Multi-function Dock

Pinout

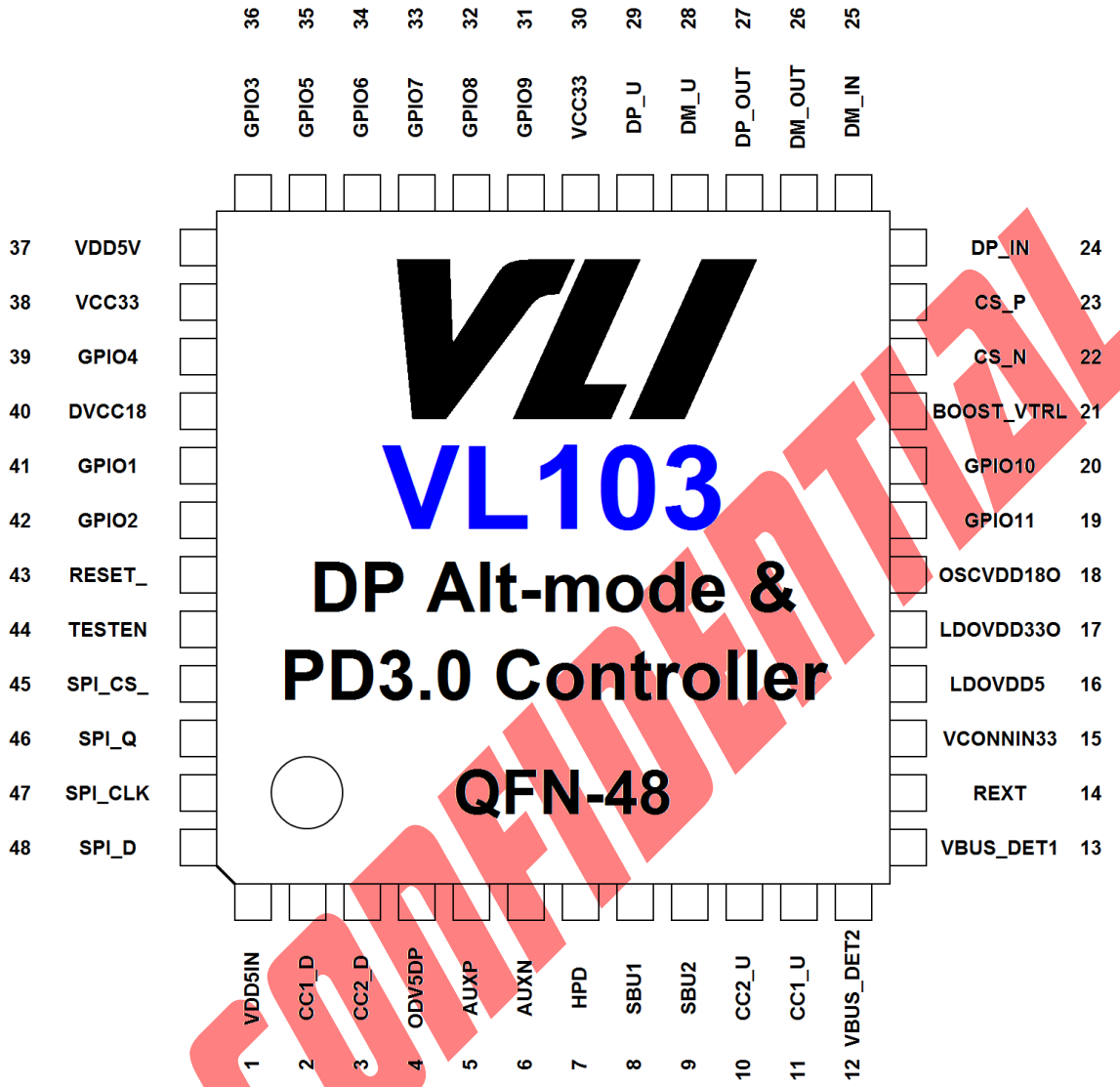


Figure 5 – VL103 QFN-48 Pin Diagram

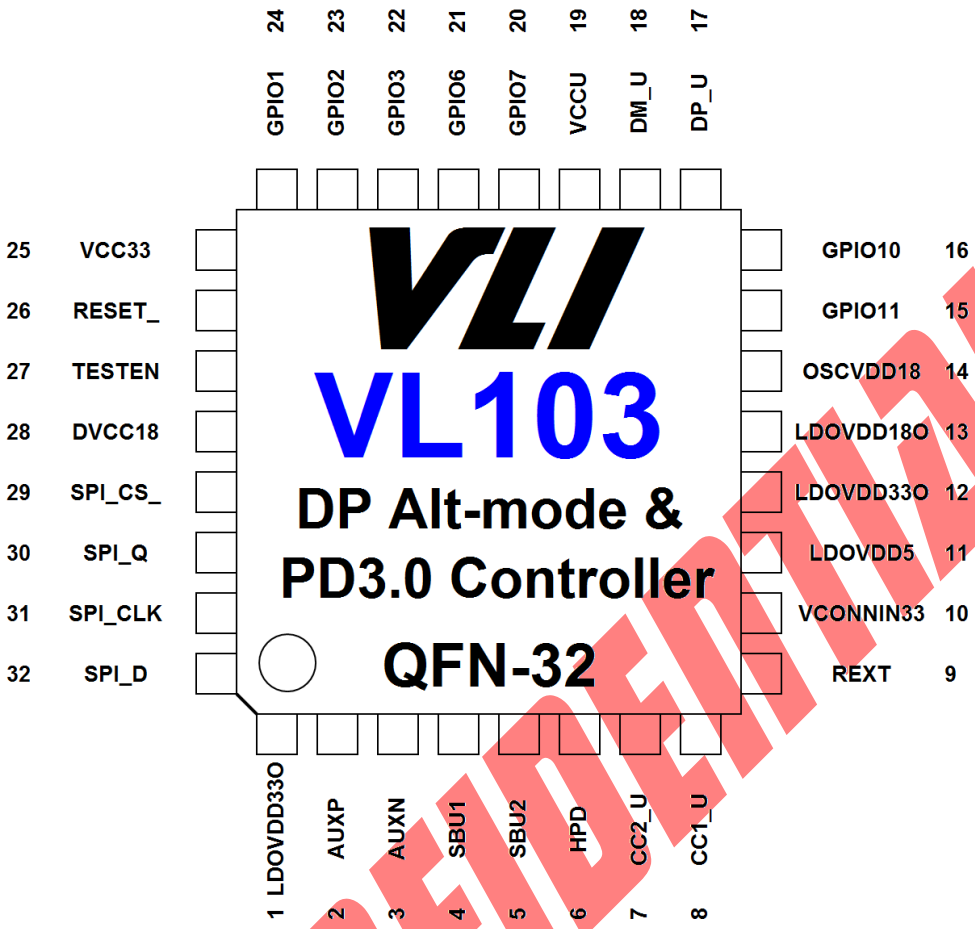


Figure 6 – VL103 QFN-32 Pin Diagram

	1	2	3	4	5	6	7	
A		VDD5V	GPIO3	GPIO7	GPIO9	DM_U		A
B	DVCC18	GPIO4	GPIO5	GPIO6	GPIO8	DP_U	CS_P	B
C	RESET_	GPIO1	VSS	VCC33	VSS	CS_N	BOOST_VTRL	C
D	SPI_CS_	TESTEN	GPIO2	VSS	OSCVDD18O	GPIO10	GPIO11	D
E	SPI_Q	SPI_CLK	VSS	VSS	VSS	LDOVDD33O	LDOVDD5	E
F	SPI_D	CC1_D	ODV5DP	CC2_U	VBUS_DET2	VCONNIN33	REXT	F
G		VDD5IN	CC2_D	HPD	CC1_U	VBUS_DET1		G
	1	2	3	4	5	6	7	

Figure 7 – VL103 VFBGA-45 Pin Diagram

Pin List

Table 1 – VL103 QFN-48 Pin List

Pin	Pin Name	Pin	Pin Name
1	VDD5IN	25	DM_IN
2	CC1_D	26	DM_OUT
3	CC2_D	27	DP_OUT
4	ODV5DP	28	DM_U
5	AUXP	29	DP_U
6	AUXN	30	VCC33
7	HPD	31	GPIO9
8	SBU1	32	GPIO8
9	SBU2	33	GPIO7
10	CC2_U	34	GPIO6
11	CC1_U	35	GPIO5
12	VBUS_DET2	36	GPIO3
13	VBUS_DET1	37	VDD5V
14	REXT	38	VCC33
15	VCONNIN33	39	GPIO4
16	LDOVDD5	40	DVCC18
17	LDOVDD33O	41	GPIO1
18	OSCVDD18O	42	GPIO2
19	GPIO11	43	RESET_
20	GPIO10	44	TESTEN
21	BOOST_VTRL	45	SPI_CS_
22	CS_N	46	SPI_Q
23	CS_P	47	SPI_CLK
24	DP_IN	48	SPI_D

Table 2 – VL103 QFN-32 Pin List

Pin	Pin Name	Pin	Pin Name
1	LDOVDD33O	17	DP_U
2	AUXP	18	DM_U
3	AUXN	19	VCCU
4	SBU1	20	GPIO7
5	SBU2	21	GPIO6
6	HPD	22	GPIO3
7	CC2_U	23	GPIO2
8	CC1_U	24	GPIO1
9	REXT	25	VCC33
10	VCONNIN33	26	RESET_
11	LDOVDD5	27	TESTEN
12	LDOVDD33O	28	DVCC18
13	LDOVDD18O	29	SPI_CS_
14	OSCVDD18	30	SPI_Q
15	GPIO11	31	SPI_CLK
16	GPIO10	32	SPI_D

Table 3 – VL103 VFBGA-45 Pin List

Pin	Pin Name	Pin	Pin Name
A2	VDD5V	D5	OSCVDD18O
A3	GPIO3	D6	GPIO10
A4	GPIO7	D7	GPIO11
A5	GPIO9	E1	SPI_Q
A6	DM_U	E2	SPI_CLK
B1	DVCC18	E3	VSS
B2	GPIO4	E4	VSS
B3	GPIO5	E5	VSS
B4	GPIO6	E6	LDOVDD33O
B5	GPIO8	E7	LDOVDD5
B6	DP_U	F1	SPI_D
B7	CS_P	F2	CC1_D
C1	RESET_	F3	ODV5DP
C2	GPIO1	F4	CC2_U
C3	VSS	F5	VBUS_DET2
C4	VCC33	F6	VCONNIN33
C5	VSS	F7	REXT
C6	CS_N	G2	VDD5IN
C7	BOOST_VTRL	G3	CC2_D
D1	SPI_CS_	G4	HPD
D2	TESTEN	G5	CC1_U
D3	GPIO2	G6	VBUS_DET1
D4	VSS		

Pin Descriptions

Signal Type Definition

Name	Type	Signal Description
Input	I	A standard input-only signal
Output	O	A standard active driver
Input/ Output	I/O	A bi-directional signal
Analog bias	A_{BIAS}	Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network
Power	PWR	A power pin
Ground	GND	A ground pin

USB-C Interface

Pin Name	QFN48	QFN32	VFBGA45	I/O	Signal Description
CC1_U	11	8	G5	I/O	Charging UFP Configuration Channel 1
CC2_U	10	7	F4	I/O	Charging UFP Configuration Channel 2
CC1_D	2	—	F2	I/O	DRP Port Configuration Channel 1
CC2_D	3	—	G3	I/O	DRP Port Configuration Channel 2
SBU1	8	4	—	I/O	Sideband Use 1
SBU2	9	5	—	I/O	Sideband Use 2

USB Billboard Interface

Pin Name	QFN48	QFN32	VFBGA45	I/O	Signal Description
DP_U	29	17	B6	I/O	D+ Data Line to USB Billboard Device
DM_U	28	18	A6	I/O	D– Data Line to USB Billboard Device

USB2.0 Interface

Pin Name	QFN48	QFN32	VFBGA45	I/O	Signal Description
DP_IN	24	—	—	I/O	D+ Data Line Connect to Downstream Facing Port
DM_IN	25	—	—	I/O	D– Data Line Connect to Downstream Facing Port
DP_OUT	27	—	—	I/O	D+ Data Line Connect to Upstream Facing Port
DM_OUT	26	—	—	I/O	D– Data Line Connect to Upstream Facing Port

DP Alt-mode Interface

Pin Name	QFN48	QFN32	VFBGA45	I/O	Signal Description
AUXP	5	2	—	I/O	DP AUX Channel Positive
AUXN	6	3	—	I/O	DP AUX Channel Negative
HPD	7	6	G4	I	DP Hot Plug Detect

SPI Interface

Pin Name	QFN48	QFN32	VFBGA45	I/O	Signal Description
SPI_CS_	45	29	D1	O	Serial Flash Chip Enable
SPI_D	48	32	F1	O	Serial Flash Data Input
SPI_Q	46	30	E1	I	Serial Flash Data Output
SPI_CLK	47	31	E2	O	Serial Flash Clock

Analog Command Block

Pin Name	QFN48	QFN32	VFBGA45	I/O	Signal Description
REXT	14	9	F7	A_{BIAS}	Connect to External Resistor (243K ohm, +/- 1% accuracy)
LDOVDD5	16	11	E7	PWR	5V Input for 5V-to-3.3V LDO
LDOVDD33O	17	12, 1	E6	PWR	3.3V Output Pin for 5V-to-3.3V LDO
LDOVDD18O	—	13	—	PWR	Analog 1.8V Power Output
OSCVDD18O	18	—	D5	PWR	Analog 1.8V Power Output
OSCVDD18	—	14	—	PWR	Oscillator Analog 1.8V Power Input
VCONNIN33	15	10	F6	PWR	3.3V Vconn Power Input
VBUS_DET1	13	—	G6	I	USB-C Charging UFP VBus Voltage Detector
VBUS_DET2	12	—	F5	I	USB-C DRP Vbus Voltage Detector
CS_P	23	—	B7	I	Current Sensing Positive Input
CS_N	22	—	C6	I	Current Sensing Negative Input
BOOST_VTRL	21	—	C7	I	Boost Voltage Control Input
VDD5IN	1	—	G2	PWR	5V Power Input for Vconn Power Output
ODV5DP	4	—	F3	O	Open-Drain IO for 5V Video Power Control

General Purpose I/O and Miscellaneous

Pin Name	QFN48	QFN32	VFBGA45	I/O	Signal Description
RESET_	43	26	C1	I	External Chip Reset
GPIO1	41	24	C2	I/O	General Purpose I/O
GPIO2	42	23	D3	I/O	General Purpose I/O
GPIO3	36	22	A3	I/O	General Purpose I/O
GPIO4	39	—	B2	I/O	General Purpose I/O
GPIO5	35	—	B3	I/O	General Purpose I/O
GPIO6	34	21	B4	I/O	General Purpose I/O
GPIO7	33	20	A4	I/O	General Purpose I/O
GPIO8	32	—	B5	I/O	General Purpose I/O
GPIO9	31	—	A5	I/O	General Purpose I/O
GPIO10	20	16	D6	I/O	General Purpose I/O
GPIO11	19	15	D7	I/O	General Purpose I/O

Test Pin

Pin Name	QFN48	QFN32	VFBGA45	I/O	Signal Description
TESTEN	44	27	D2	I	Test Mode Enable; Internal pull down Do not connect for normal operation.

Power and Ground

Pin Name	QFN48	QFN32	VFBGA45	I/O	Signal Description
VDD5V	37	—	A2	PWR	E-fuse Power Input, Connecting to 3.3V in Normal Use
VCC33	30, 38	25	C4	PWR	Digital 3.3V IO Power Input
VCCU	—	19	—	PWR	Analog 3.3V Power Input
DVCC18	40	28	B1	PWR	Digital 1.8V Core Power Input
VSS	EPAD	EPAD	C3, C5, D4, E3, E4, E5	GND	Ground

Electrical Specification

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-55	125	°C	—
V_{DD33}	3.3V Power Input Voltage	-0.5	3.69	V	—
V_{DD50}	5V Power Input Voltage	-0.5	5.5	V	—
V_O	Output Voltage at any output	-0.5	VCC+ 0.5	V	—
V_{ESD}	Electrostatic Discharge	-2	2	kV	Human Body Model
Θ_{JC}	Thermal resistance between junction and case	QFN32 for 4-layer PCB: 16.9 QFN48 for 4-layer PCB: 14.6 BGA45 for 4-layer PCB: 23.9		°C/W	4L PCB definitions follow JESD51-7
Θ_{JA}	Thermal resistance between junction and ambient	QFN32 for 4-layer PCB: 33.5 QFN48 for 4-layer PCB: 29.9 BGA45 for 4-layer PCB: 54.0		°C/W	
P_D	Max Power Dissipation	—	47.5	mW	—

Note:
1. Stress above conditions may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described.
2. About thermal factors, T_A is the concerned ambient temperature, and
   $\Theta_{CA} = \theta_{JA} - \theta_{JC}$
   $T_J = \theta_{JA} * P_D + T_A$
   $T_C = \theta_{CA} * P_D + T_A$

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
LDOVDD5	5V to 3.3V LDO 5V Power Input	4.5	5	5.5	V
VCONNIN33	3.3V Vconn power input	3.0	3.3	3.6	V
V_{CC33}	Digital IO power 3.3V	3.0	3.3	3.6	V
DV_{CC18}	Digital Core power 1.8V	1.62	1.8	1.98	V
DGND	Ground	—	0	—	V
T_A	Ambient Temperature	0		70	°C
T_J	Junction Temperature	0		125	°C

General IO DC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.30	0.8	V	—
V_{IH}	Input High Voltage	2.0	3.6	V	—
V_{OL}	Output Low Voltage	—	0.4	V	IOL=15.8mA
V_{OH}	Output High Voltage	2.4	—	V	IOH=26.5mA
I_{IL}	Input Leakage Current	—	+/-10	µA	0<VIN<VCC
I_{OZ}	Tristate Leakage Current	—	+/-10	µA	0<VOUT<VCC

Internal 3.3V to 1.8V LDO Regulator

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	3.0	3.3	3.6	V	
Output Voltage	1.71	1.8	1.89	V	
Max. Output Current			100	mA	
Output Voltage Tolerance		+/- 5%			

Internal 5V to 3.3V LDO Regulator

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	4.5	5.0	5.5	V	
Output Voltage	3.135	3.3	3.465	V	
Max. Output Current			100	mA	
Output Voltage Tolerance		+/- 5%			

PD BMC DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
$V_{BMCSWING}$	Voltage Swing	1.05	1.2	V	—
Z_{BMCDRV}	Drive Output Resistance	33	75	Ω	—
T_{BMCR}	Rise Time	300		ns	—
T_{BMCF}	Fall Time	300		ns	—

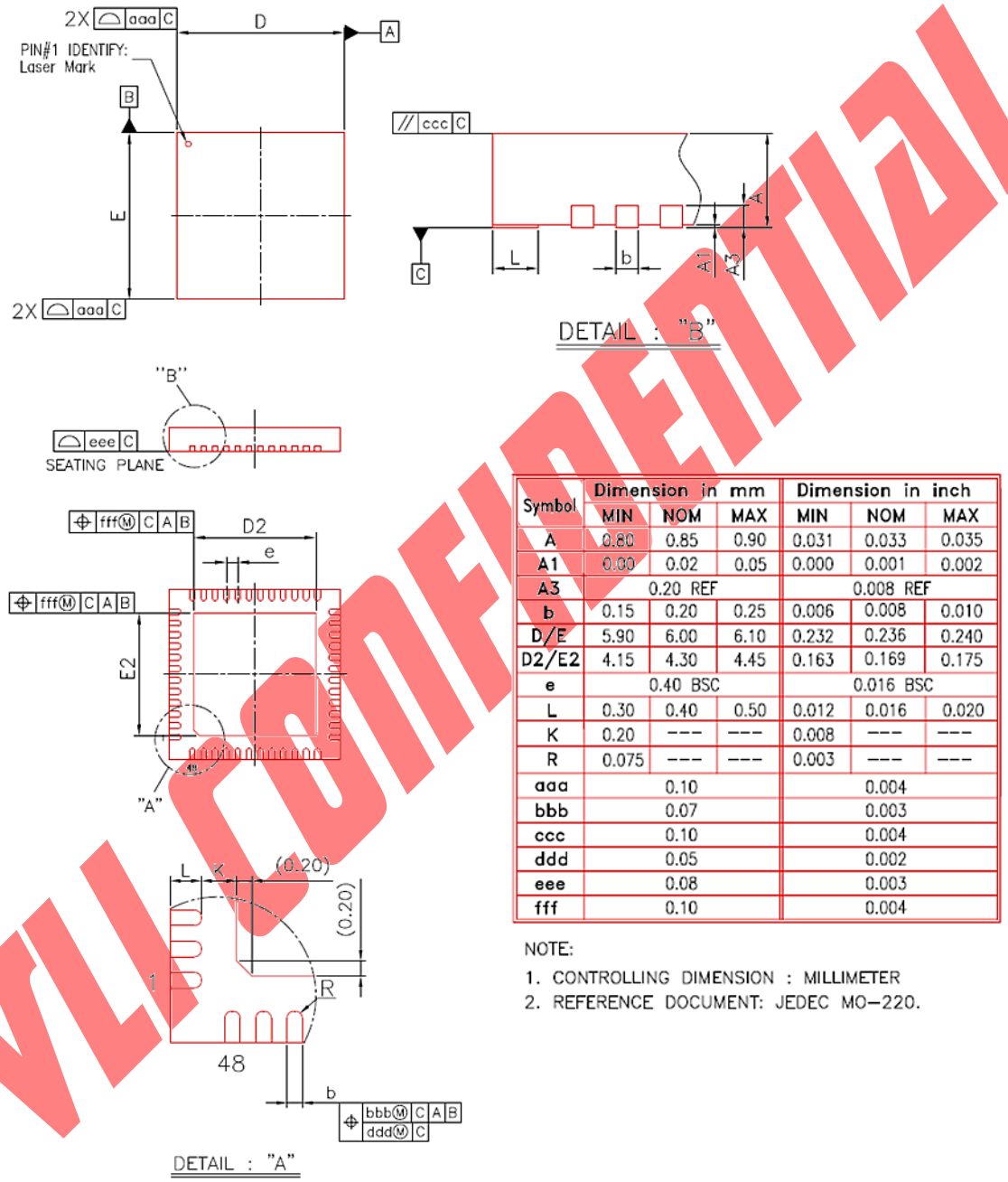
USB Full Speed DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{IH}	High state input level	2.0		V	—
V_{IHZ}	High-z state input level	2.7	3.6	V	—
V_{IL}	Low state input level		0.8	V	—
V_{DI}	Differential input sensitivity	0.2		V	—
V_{CM}	Differential common mode	0.8	2.5	V	—
V_{OL}	Low state output level	0.0	0.3	V	—
V_{OH}	High state output level	2.8	3.6	V	—
V_{CRS}	Output signal crossover voltage	1.3	2.0	V	—
R_{PU}	Bus pull-up resistor	1.425	1.575	KΩ	—
Z_{DRV}	Driver output resistance	28	44	Ω	—
T_{FR}	Full-speed Rise Time	4	20	ns	—
T_{FF}	Full-speed Fall Time	4	20	ns	—

Package Mechanical Specifications

QFN-48 Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	250	°C
Max Time within 5°C of Tp	30	seconds



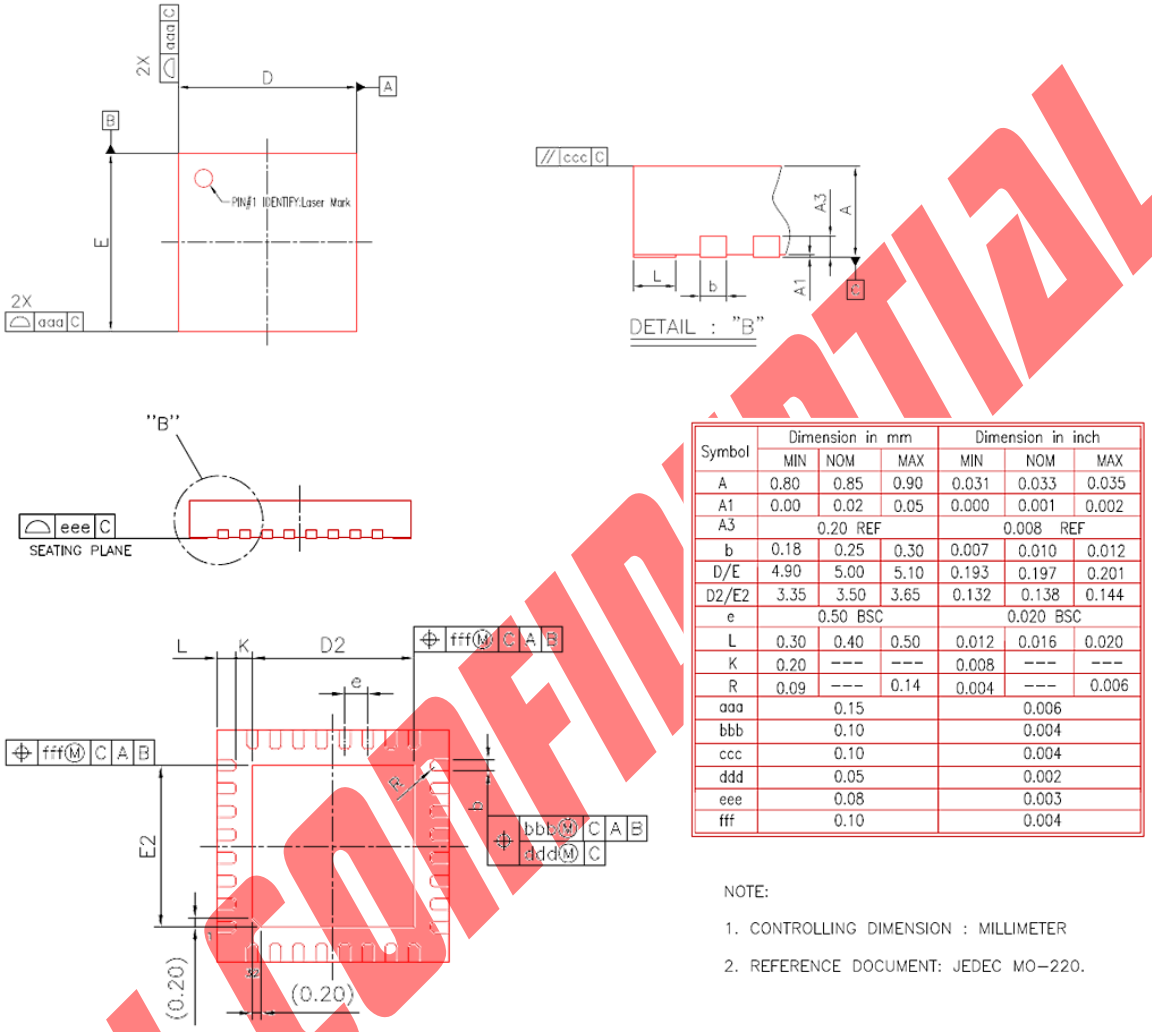
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
D2/E2	4.15	4.30	4.45	0.163	0.169	0.175
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 8 – QFN 48L 6x6x0.85 mm Mechanical Specification

QFN-32 Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	250	°C
Max Time within 5°C of Tp	30	Seconds



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	4.90	5.00	5.10	0.193	0.197	0.201
D2/E2	3.35	3.50	3.65	0.132	0.138	0.144
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.09	---	0.14	0.004	---	0.006
aaa		0.15			0.006	
bbb		0.10			0.004	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	
fff		0.10			0.004	

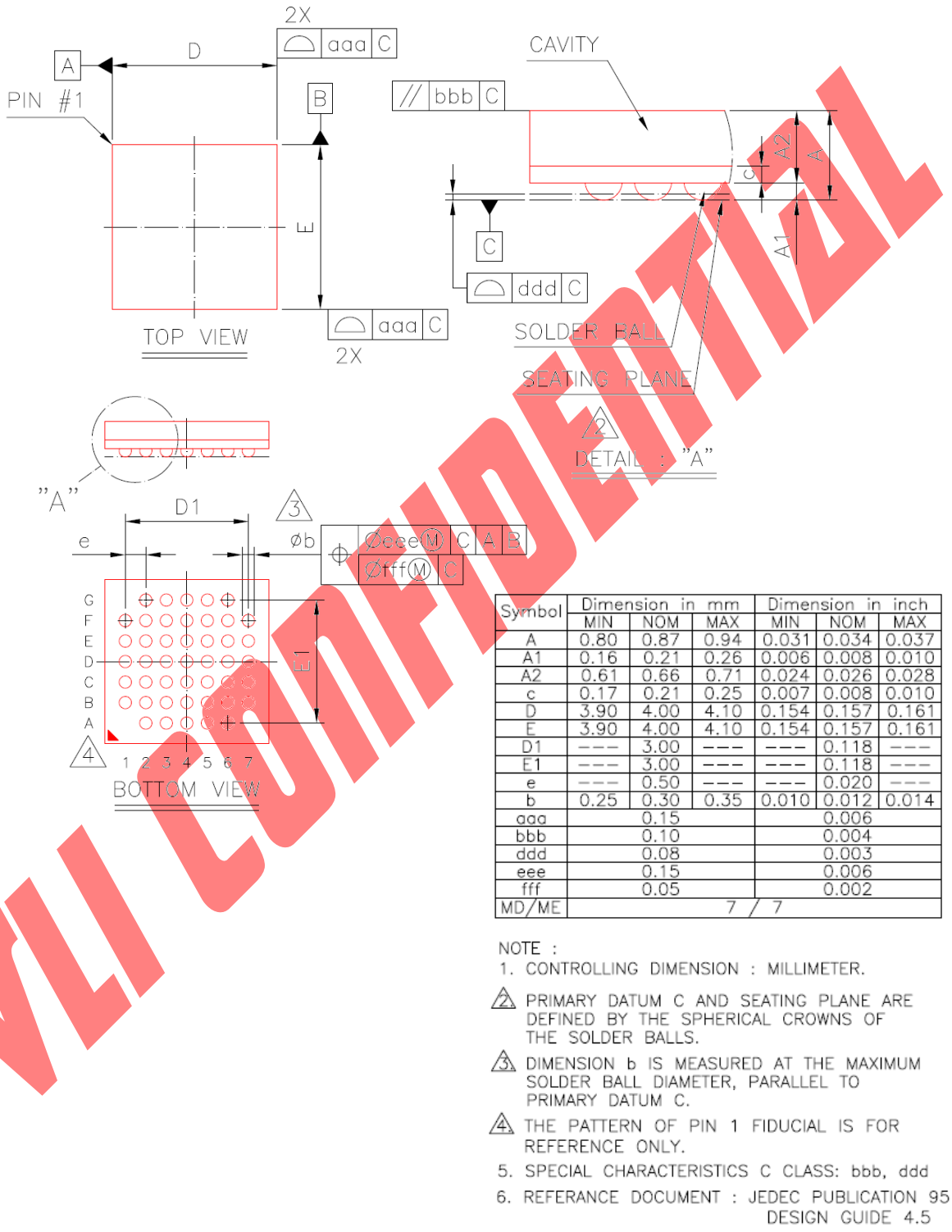
NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 9 – QFN 32L 5x5x0.85 mm Mechanical Specification

VFBGA-45 Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	260	°C
Max Time within 5°C of Tp	30	Seconds



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.87	0.94	0.031	0.034	0.037
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.61	0.66	0.71	0.024	0.026	0.028
c	0.17	0.21	0.25	0.007	0.008	0.010
D	3.90	4.00	4.10	0.154	0.157	0.161
E	3.90	4.00	4.10	0.154	0.157	0.161
D1	---	3.00	---	---	0.118	---
E1	---	3.00	---	---	0.118	---
e	---	0.50	---	---	0.020	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.08			0.003	
eee		0.15			0.006	
fff		0.05			0.002	
MD/ME		7 / 7				

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
5. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd
6. REFERANCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5

Figure 10 – VFBGA 45L 4x4x0.87 mm Mechanical Specification

Package Top Side Marking

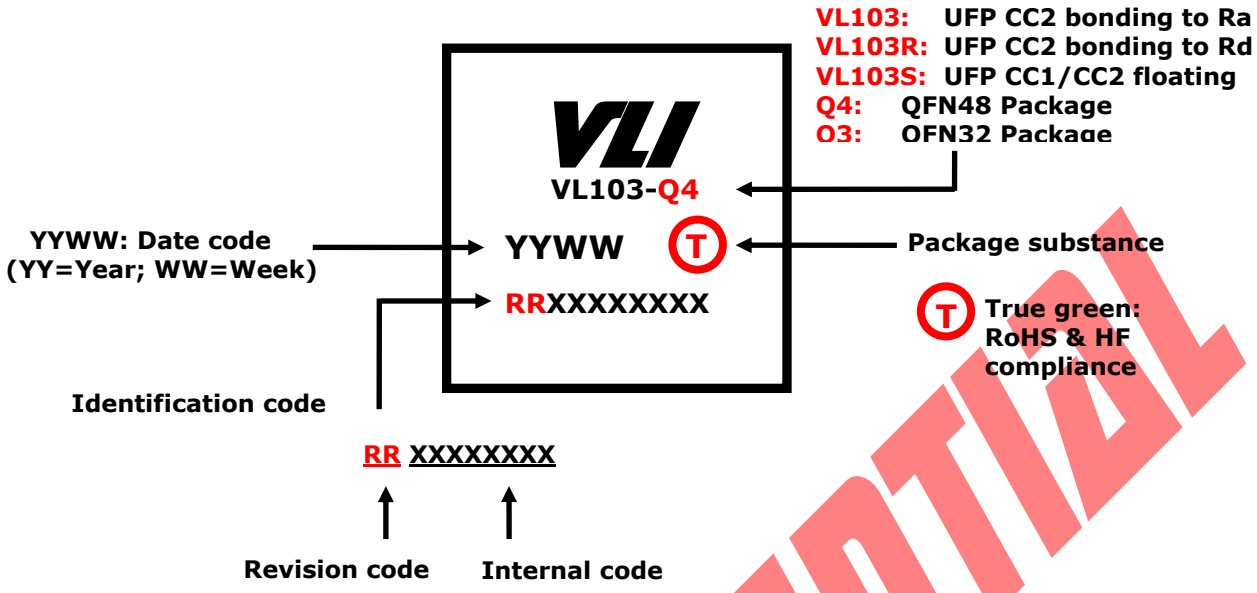


Figure 11 – VL103 QFN Package Top Side Marking

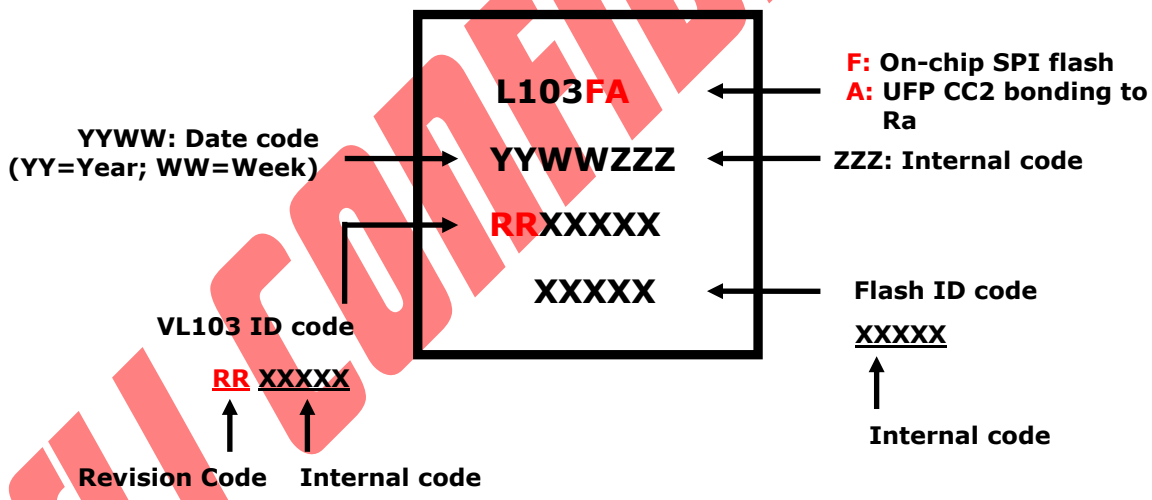


Figure 12 – VL103 VFBGA Package Top Side Marking

Ordering Information

Please contact VIA Labs sales representative or distributor in your region for ordering part number details.

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